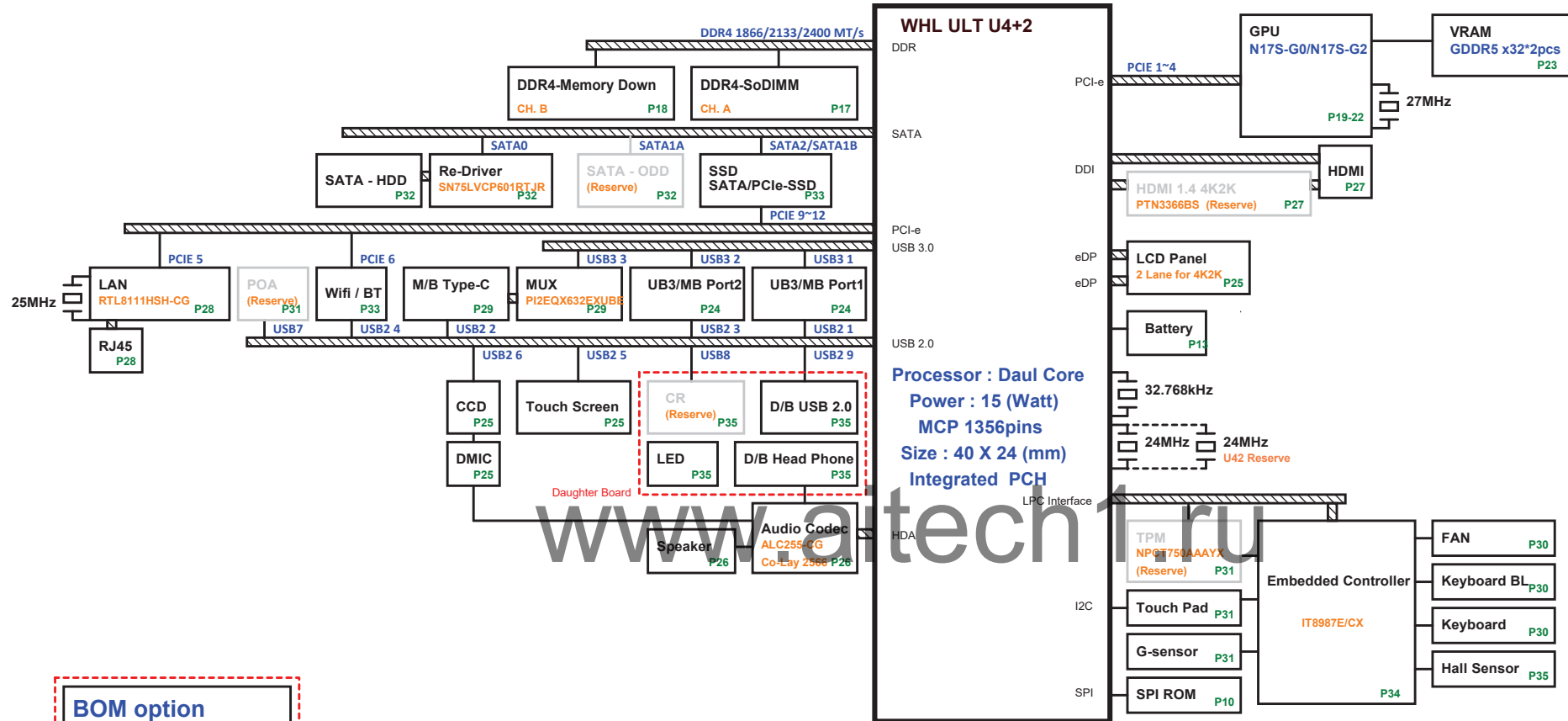


ZAW Whiskey Lake series Platform Block Diagram (DIS/UMA)

01

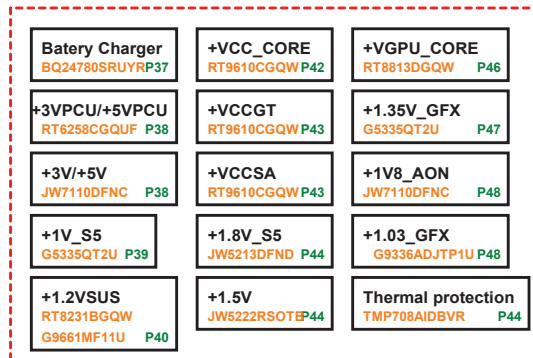


BOM option

IV@ : UMA
 EV@ : DIS
 TPC@ : Type-C function
 TPC_N@ : No Type-C function
 TSI@ : Touch screen I2C
 TPM@ : Trusted Platform Module
 PBA@ : Finger Print on touch pad
 KBL@ : Keyboard back light
 GS@ : G-Sensor function
 GS_N@ : No G-Sensor function
 SSD@ : Solid State Disk
 ODD@ : Optical Disc Drive
 EMC@ : eMMC function
 RAM@ : On Board Memory
 SP@ : Power & VGA
 HDD_R@ : Hard Disc Redriver
 HDD_N@ : NO Hard Disc Redriver
 CNV@ : Intel WIFI
 CNV_N@ : NO Intel WIFI
 HDMI_R@ : HDMI Redriver
 HDMI_N@ : No HDMI Redriver
 Debug@ : for Debug Card
 255@ : Codec 255
 256@ : Codec 256

FOR15~17@ : Panel 15 or 17 inch
 FOR14@ : Panel 14 inch

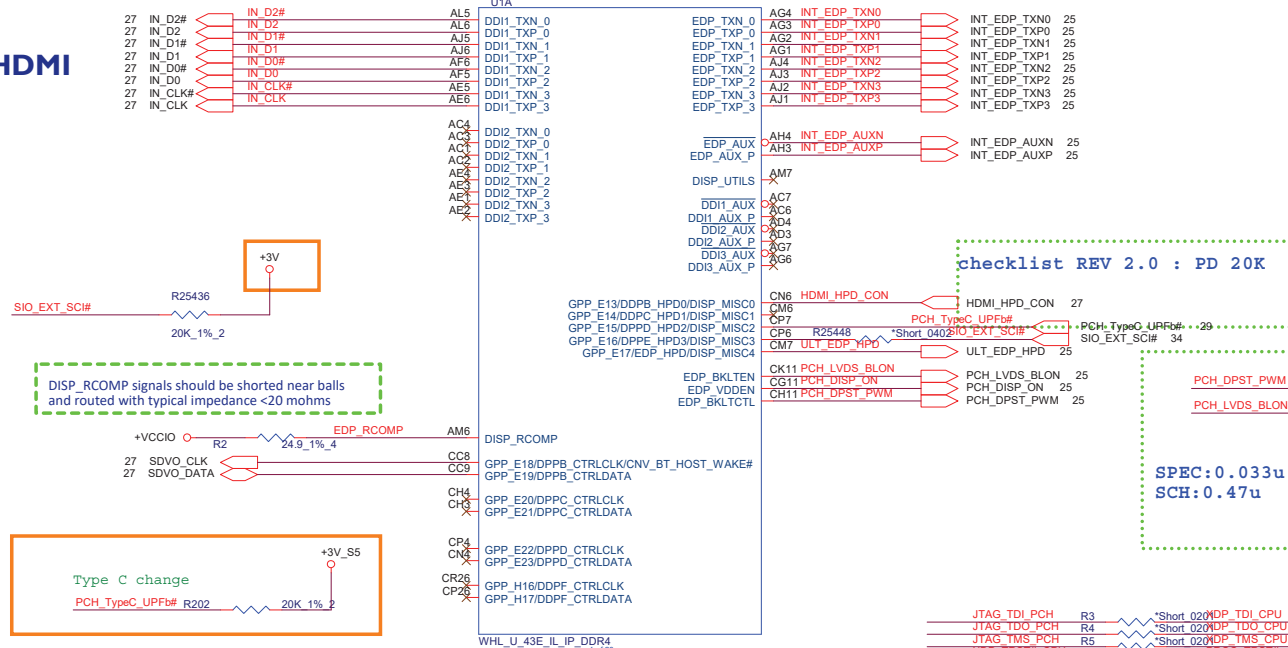
Power solution



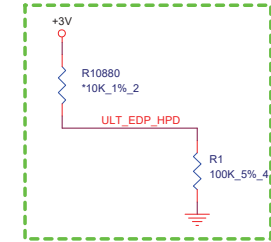
PCB 8L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1
 LAYER 4 : SVCC
 LAYER 5 : IN2
 LAYER 6 : IN3
 LAYER 7 : SGND
 LAYER 8 : BOT

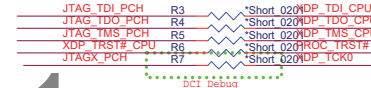
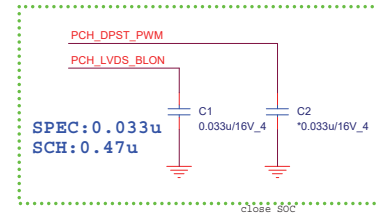
HDMI



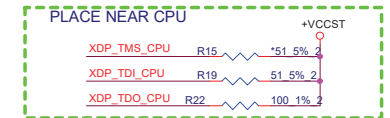
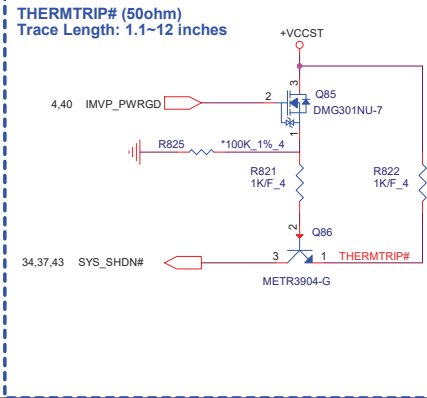
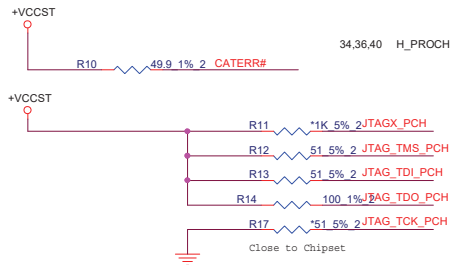
Reserve EDP_HPD opposites circuit!



checklist REV 2.0 : PD 20K



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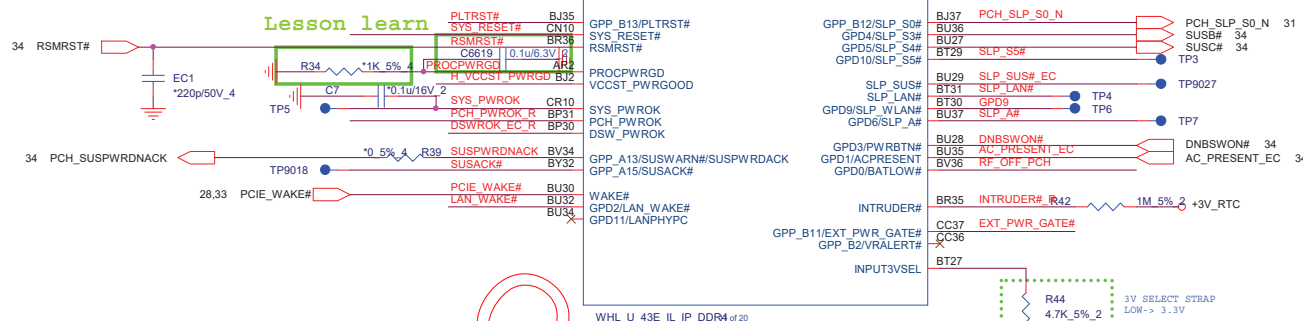
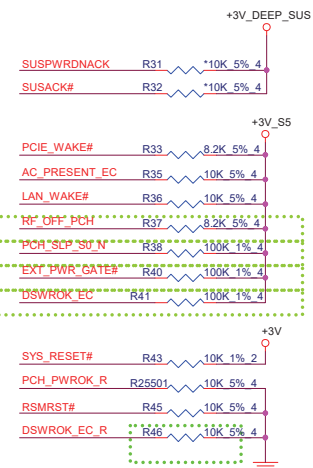
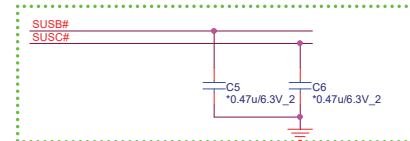


Quanta Computer Inc.

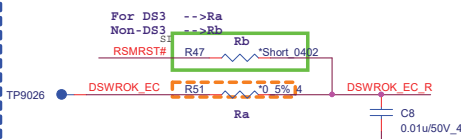
PROJECT : ZAW

| | | |
|-------|------------------------------|---------------|
| Size | Document Number | Rev |
| | KBL-U 1/15 eDP/DDI/MISC | 1A |
| Date: | Wednesday, February 27, 2019 | Sheet 2 of 48 |

PCH Pull-high/low(CLG)

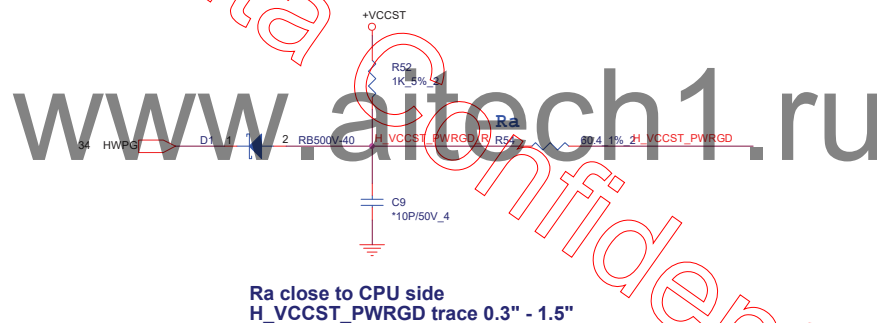
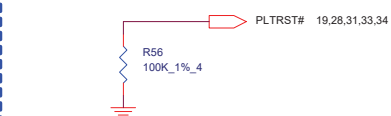


For DS3 Sequence

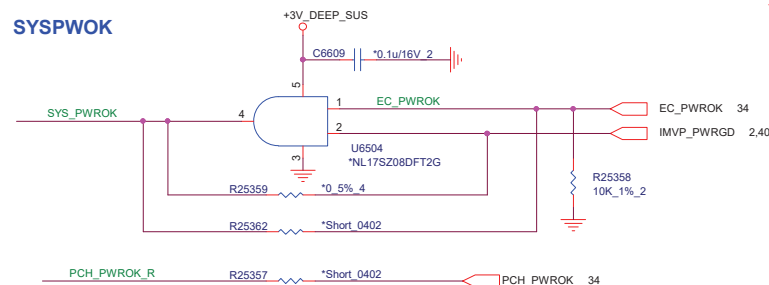


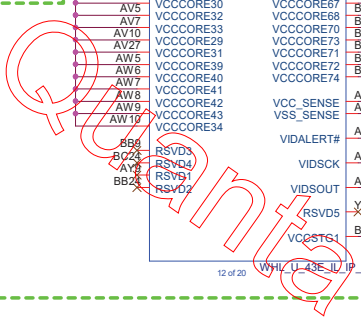
PLTRST#(CLG)

Check Rise/Fall time less than 100ns



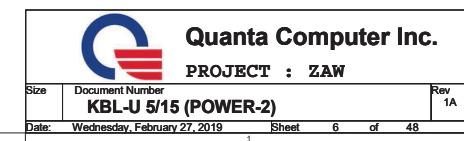
SYSPWOK

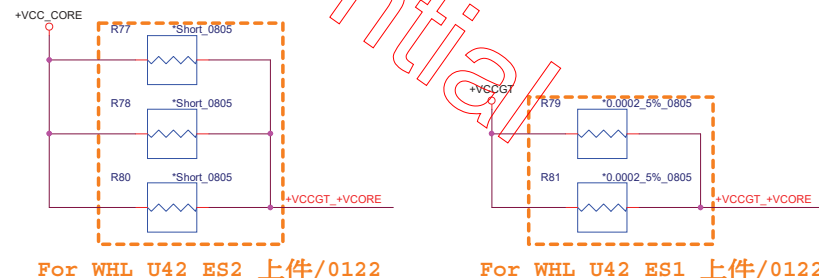
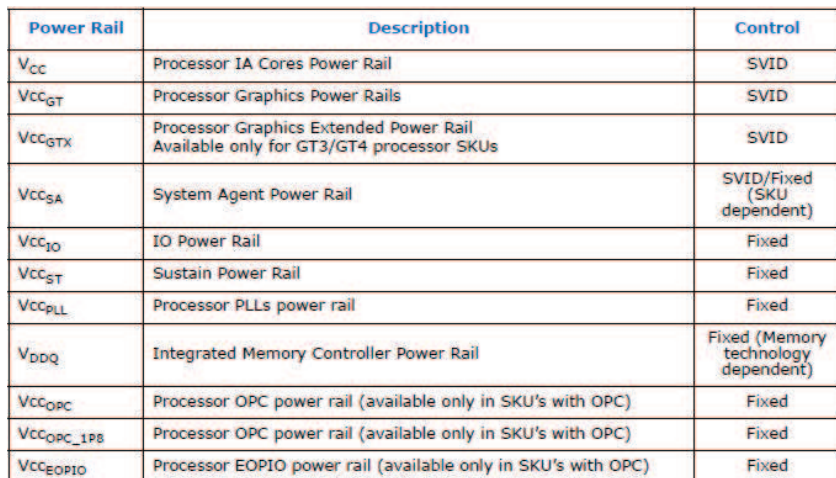


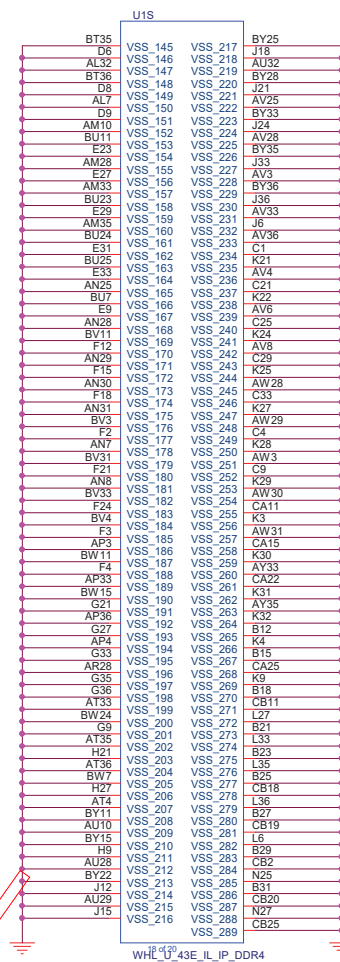
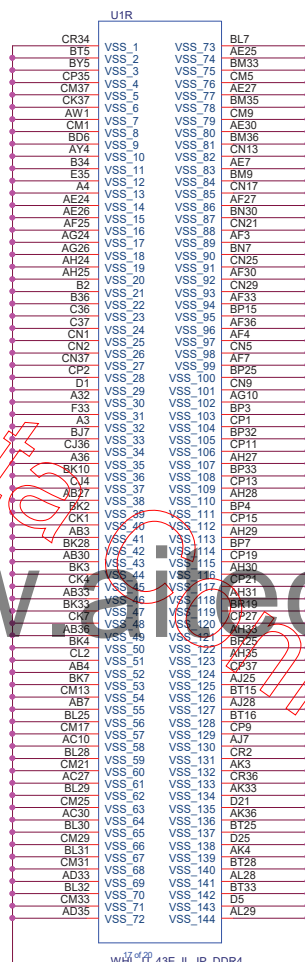
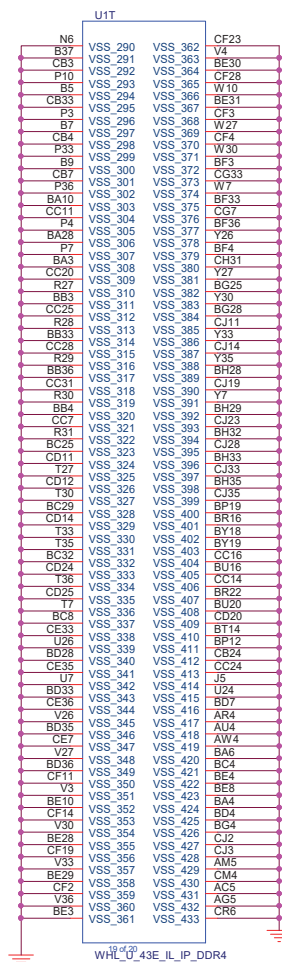
5

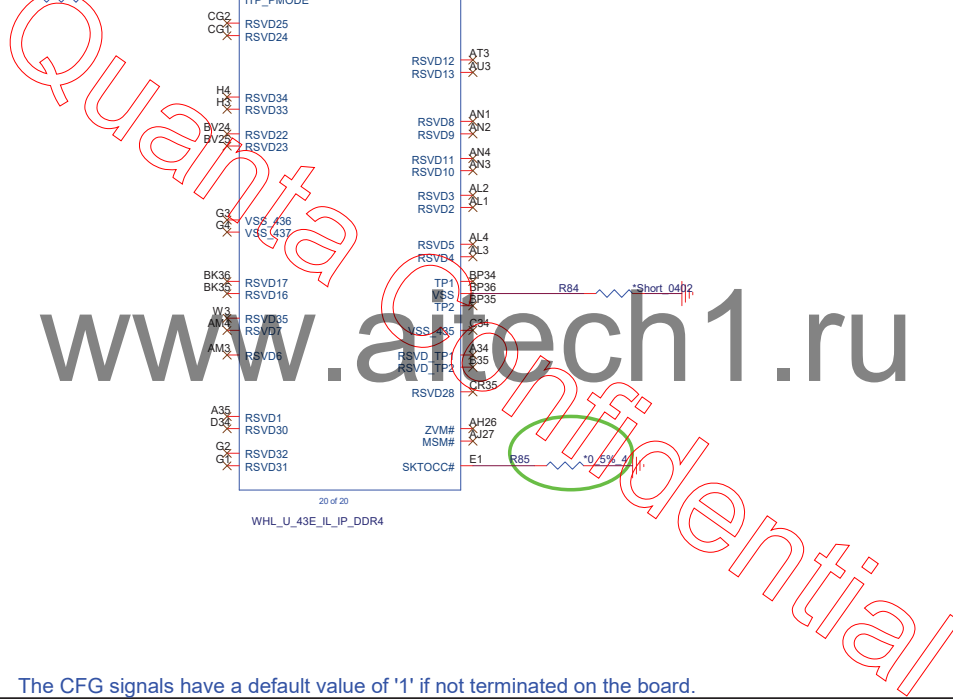
**CLOSE TO CPU
PLACE THE PU RESISTORS**













| | 1 | 0 | Circuit |
|--|---|--|--|
| CFG3 (Physical Debug Enable) DFX Privacy | Disable: | Enable: Set DFX Enable in DFX interface MSR |  |
| CFG4 (DP Presence Strap) | Disable: No physical DP attached to eDP | Enable: An ext DP device is connected to eDP |  |
| | | | |

| | | | | |
|-------------|------|------|----|---|
| SMB_PCH_CLK | R95 | 2.2K | 5% | 2 |
| SMB_PCH_DAT | R97 | 2.2K | 5% | 2 |
| SMB_ME0_CLK | R99 | 2.2K | 5% | 2 |
| SMB_ME0_DAT | R101 | 2.2K | 5% | 2 |
| SMB_ME1_CLK | R103 | 2.2K | 5% | 2 |
| SMB_ME1_DAT | R104 | 2.2K | 5% | 2 |

| Vender | | Size | P/N | |
|----------|------------|------|-------------|-------------------|
| Kabylake | MXIC | 16M | AKE3DZN0Z03 | MX25L12873FM2I-10 |
| POA 3.3V | Winbond | 16M | AKE3DF-KN01 | W25Q128JVSQI |
| | GigaDevice | 16M | AKE3DZN0Q02 | GD25B127DSIGR |

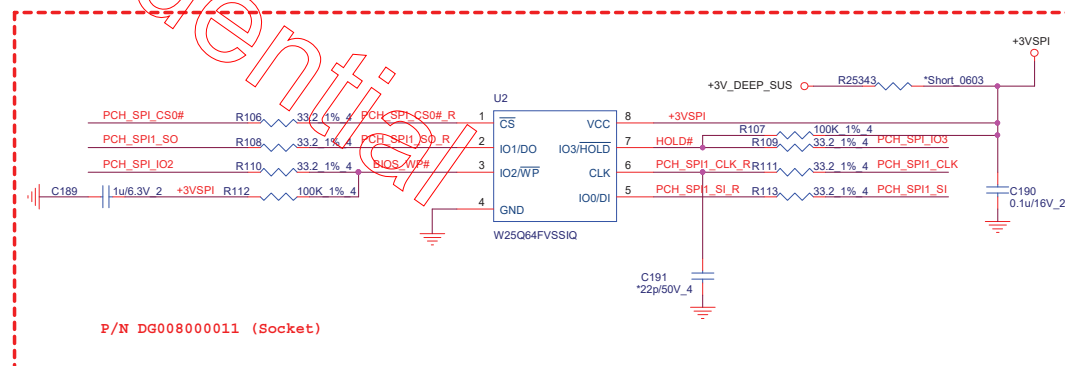
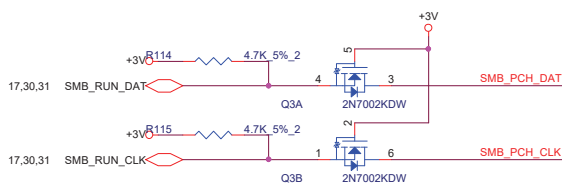
| | |
|------|----------------|
| TP14 | PCH_SPI_CS0#_R |
| TP15 | PCH_SPI_CLK_R |
| TP16 | PCH_SPI_SI_R |
| TP17 | PCH_SPI_SO_R |
| TP18 | BIOS_WP# |
| TP19 | HOLD# |

TP_size TP2675

| | | | |
|----|----------------|--|----------------|
| 34 | PCH_SPI_CS0#_R | | PCH_SPI_CS0#_R |
| 34 | PCH_SPI1_CLK_R | | PCH_SPI1_CLK_R |
| 34 | PCH_SPI1_SI_R | | PCH_SPI1_SI_R |
| 34 | PCH_SPI1_SO_R | | PCH_SPI1_SO_R |

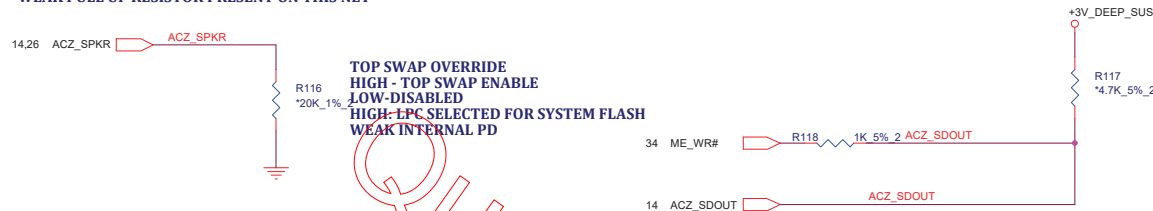
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

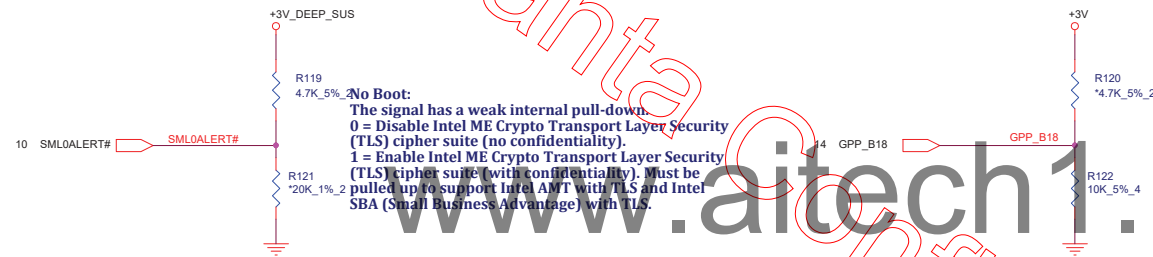


Functional Strap Definitions

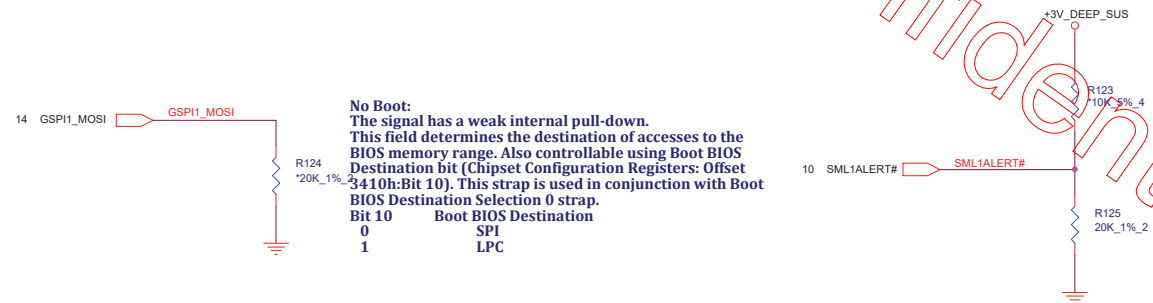
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

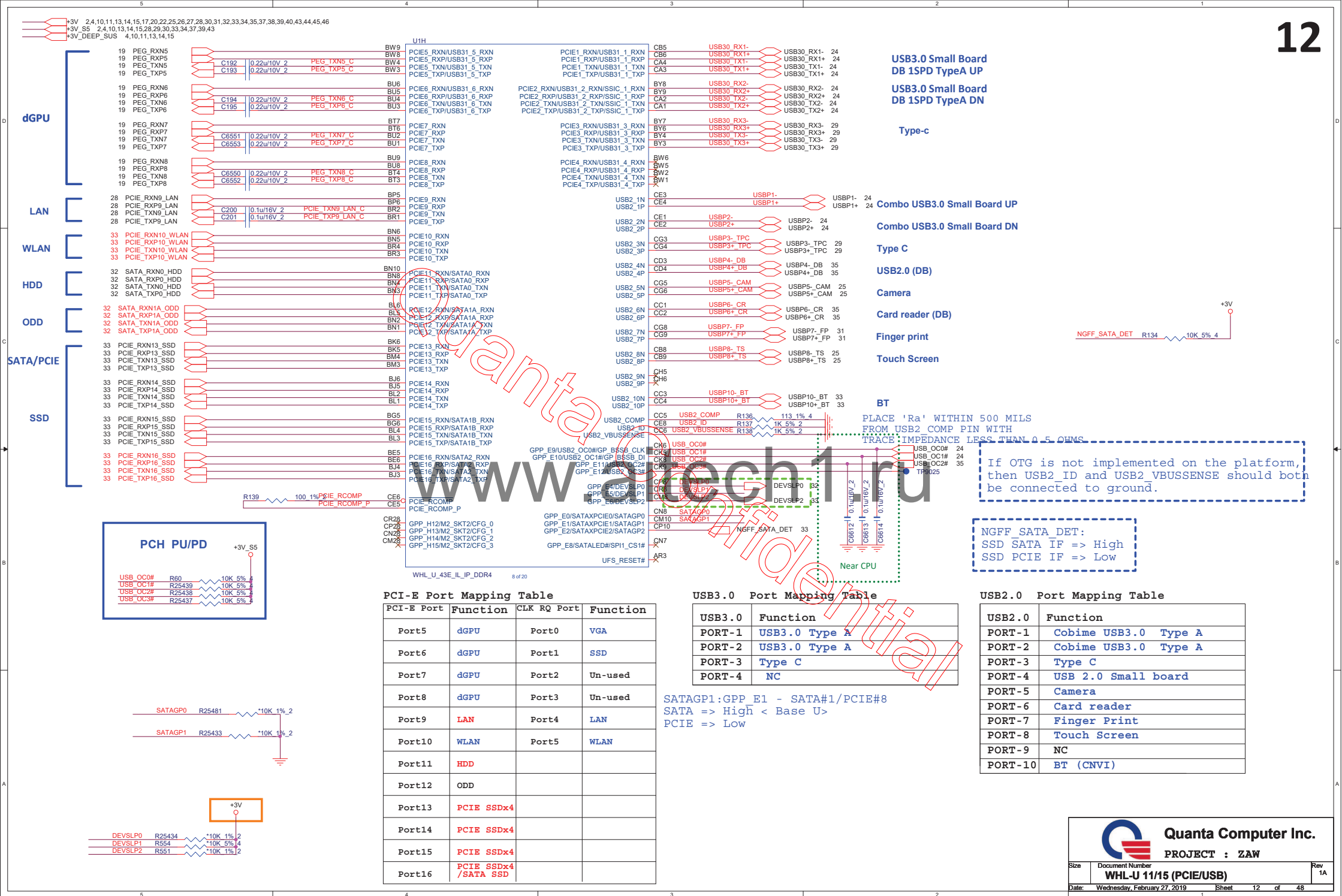


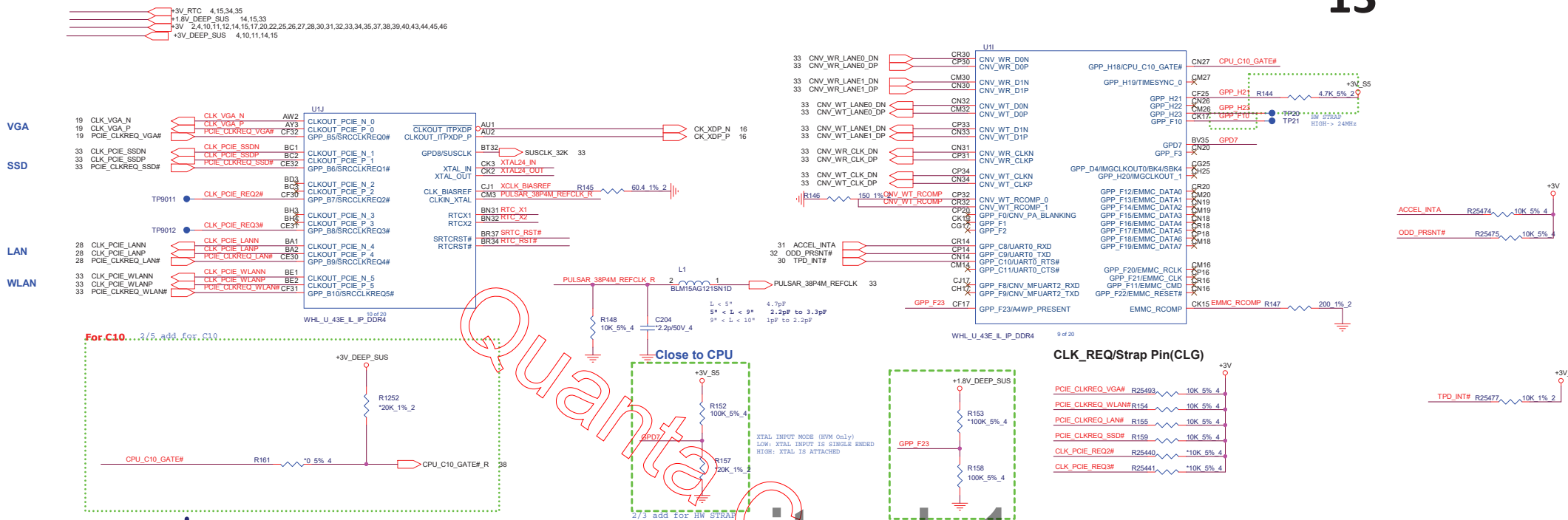
Quanta Computer Inc.

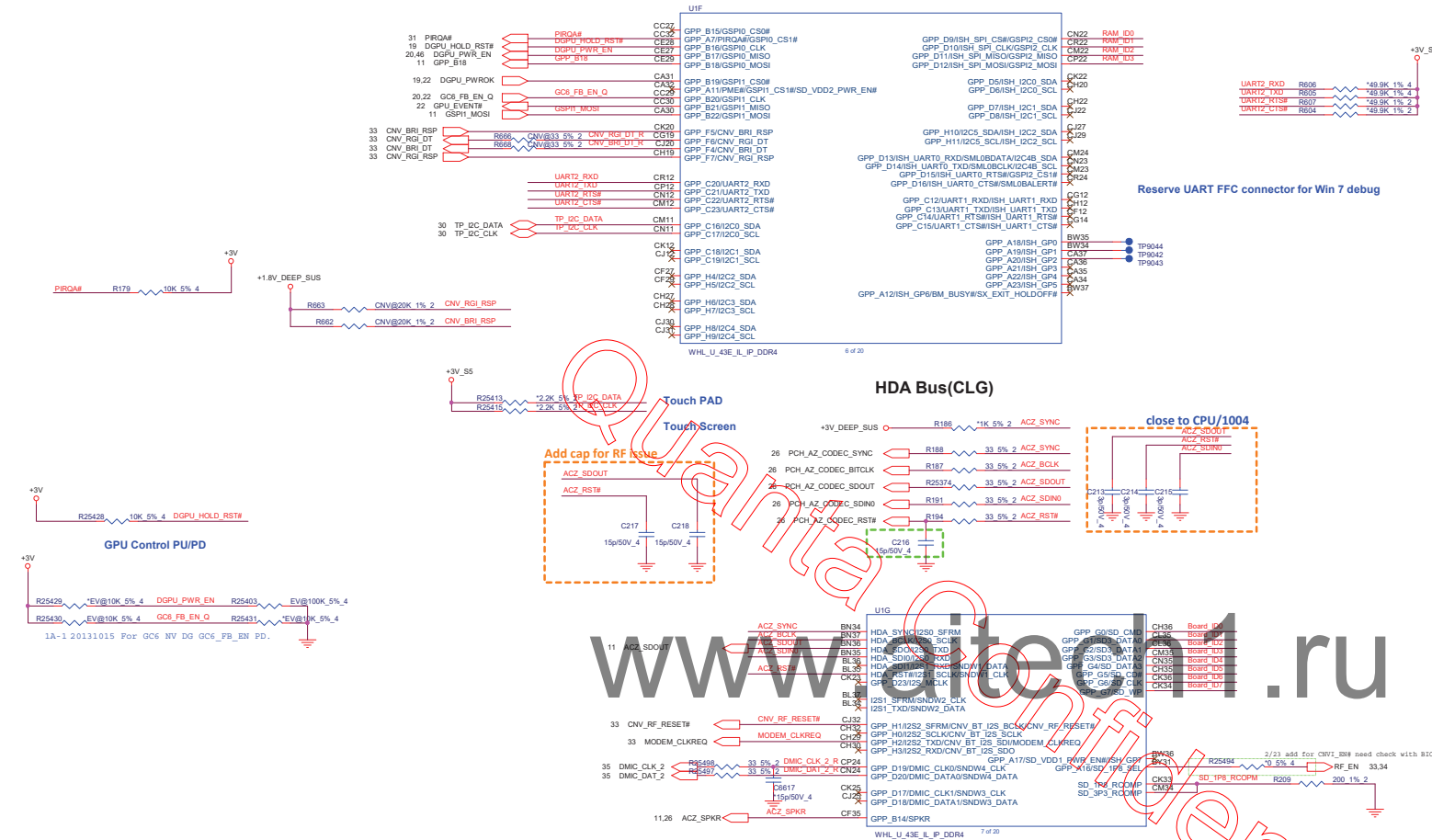
PROJECT : ZAW

| Size | Document Number | Rev |
|------|-------------------------|-----|
| | KBL-U 10/15(HDA) | 1A |

Date: Wednesday, February 27, 2019 Sheet 11 of 48







RAM ID

Diagram illustrating the RAM ID pins and their connections. The RAM ID pins (R25376, R25379, R25380, R25385) are connected to the SPB10K 5% 4 and RAM ID1, ID2, ID3 pins. The RAM ID pins are connected to R25381, R25382, R25383, and R25384, which are also connected to SPB10K 5% 4. A +3V_5S supply is shown at the top right.

| ID3 | ID2 | ID1 | ID0 | Vendor | Vendor PN | Quanta PN |
|-----|-----|-----|-----|--------------------------|----------------------|-------------|
| 0 | 0 | 0 | 0 | Hynix 8Gb | H5AN8G6NCJR-VKC | AKD5QGSTW13 |
| 0 | 0 | 0 | 1 | Micron 8Gb | MT40A512M16LY-075-E | AKD5LZSLT24 |
| 0 | 0 | 1 | 0 | Micron 8Gb | MT40A512M16TB-062-EJ | AKD5QGSTL23 |
| 1 | 1 | 1 | 1 | With out on board memory | | |

Board_ID0

Board_ID1

+3V_SS

| | Low | High |
|-----------|---------------------------|-----------------------------------|
| BOARD_ID0 | Non eMMC | eMMC |
| BOARD_ID1 | HDMI_N@ | HDMI_R@ |
| BOARD_ID2 | Non G-sensor(GS_N@) | G-sensor(GS@) |
| BOARD_ID3 | Non TPM(TPM_N@) | TPM(TPM@) |
| BOARD_ID4 | Non Touch panel | Touch panel (Control by Cable) |
| BOARD_ID5 | Non Type-C(TPC_N@) | Type-C(TPC@) |
| BOARD_ID6 | Single MIC(Cable control) | Dual MIC (DMIC@) |
| BOARD_ID7 | Reserved (Default) | Reserve |

DGPW_PW_CTRL#

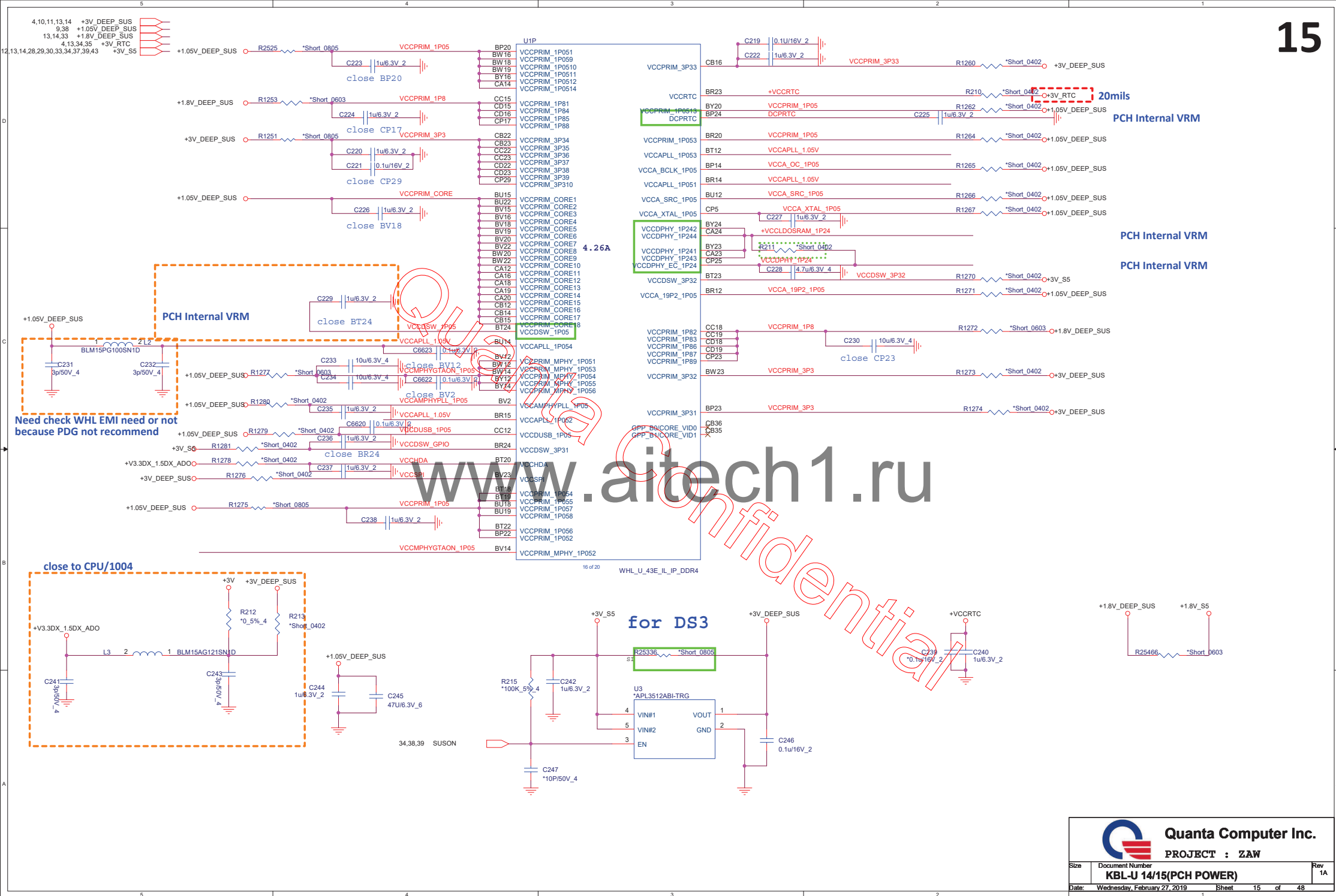
| | |
|------|---|
| high | UMA Only |
| low | GPO power is control by PWM GPIO (Discrete, SG or Optimize) |

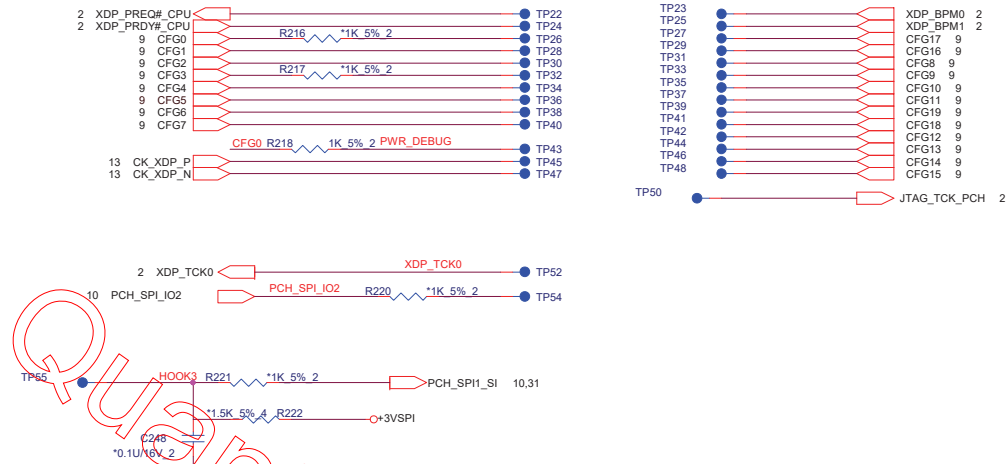
2 DGPW_PW_CTRL#

R25375 EVB100K_1%_4 DGPW_PW_CTRL# R25376 R25376 VBIAS10K_4 EVB10K_1%_2

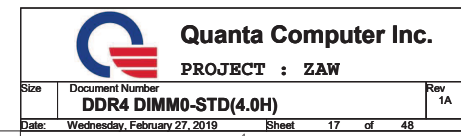
DGPW_PWROK PD on GPU side

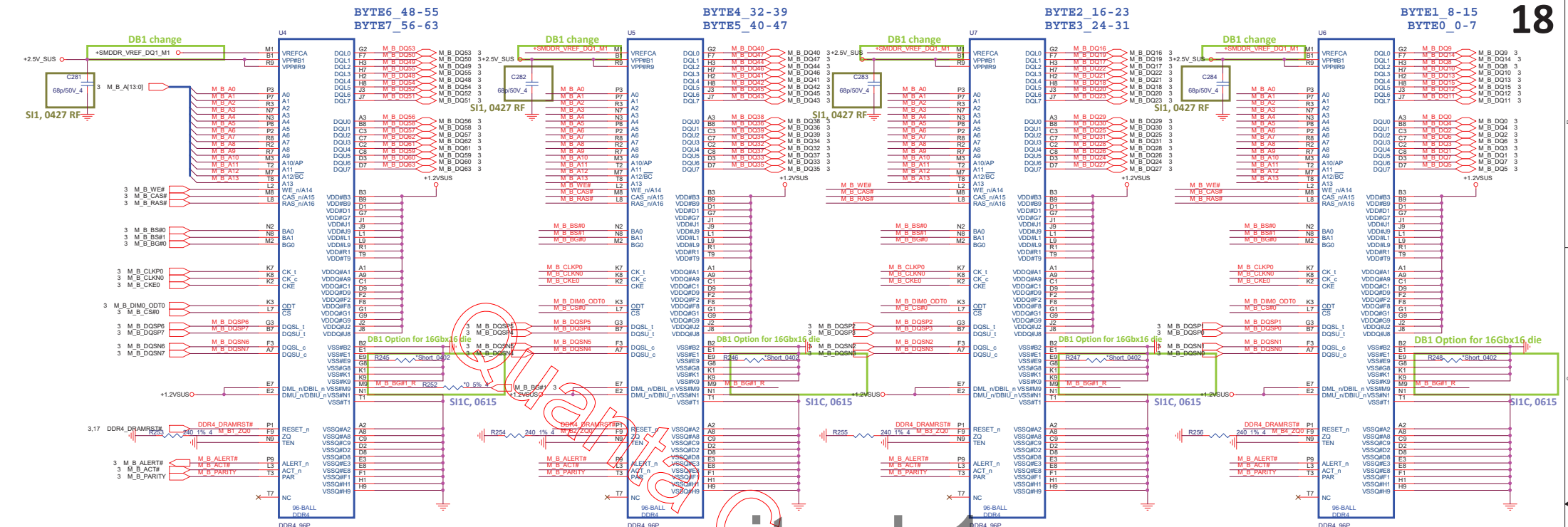
| | DGPW_PW_CTRL# | VGA H/W Signal | Setup Menu | |
|-------------|---------------|----------------|------------|----------|
| UMA Only | 1 | UMA | Hidden | UMA boot |
| sg/Optimize | 0 | GPU | Hidden | GPU boot |



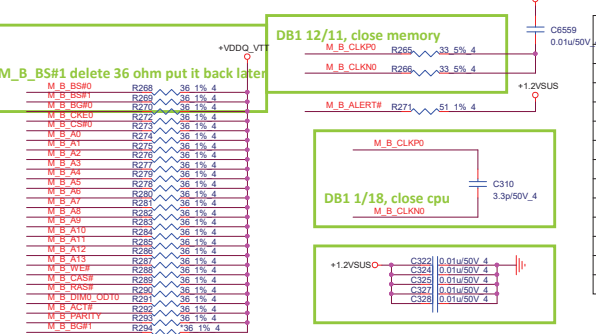


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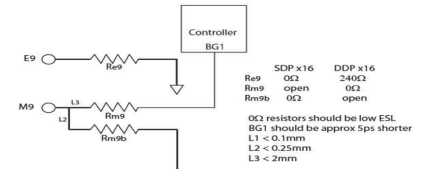




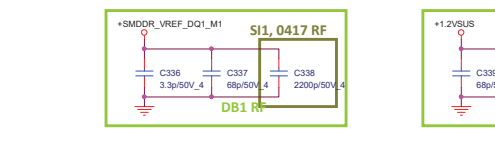
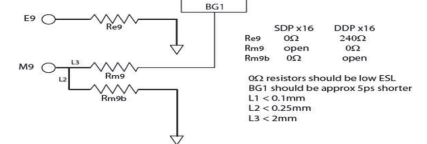
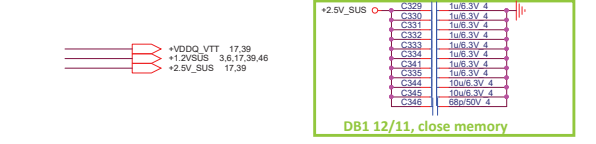
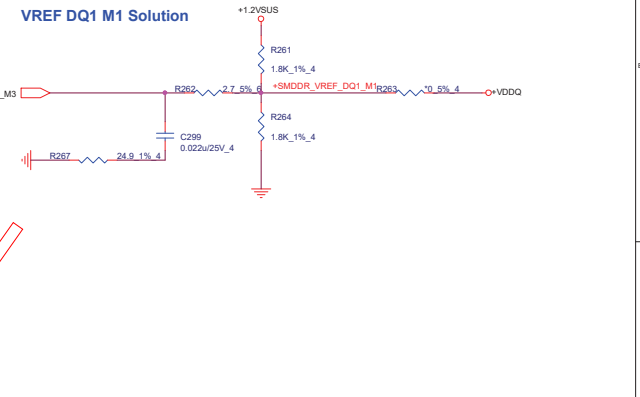
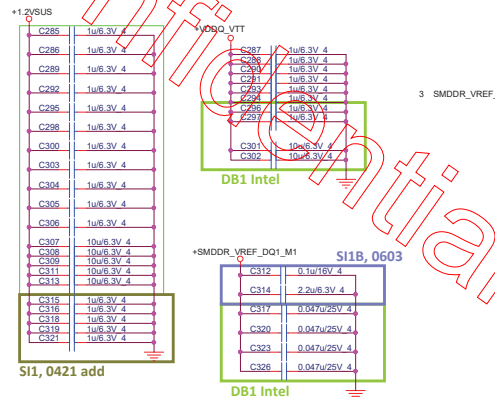
| Vendor | P/N | Vendor | P/N |
|---------|-------------|----------------------|-----|
| MIC 16G | AKDS5G0TL00 | MT40A0G1G16BA-083E:A | |
| Elpida | | | |
| SAMSUNG | | | |

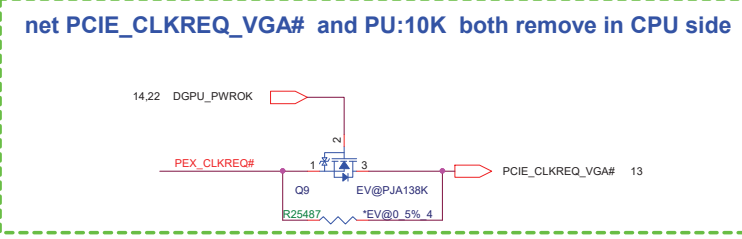
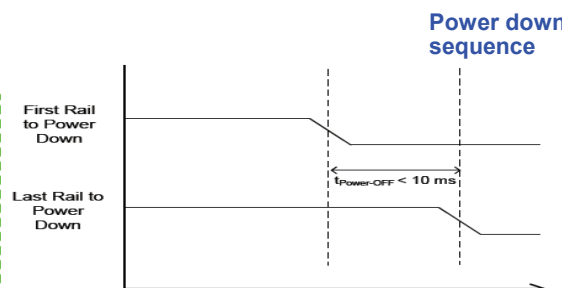
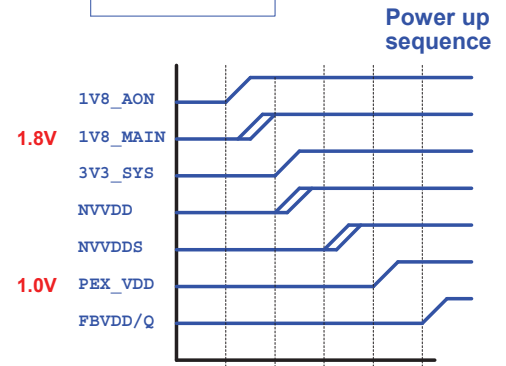
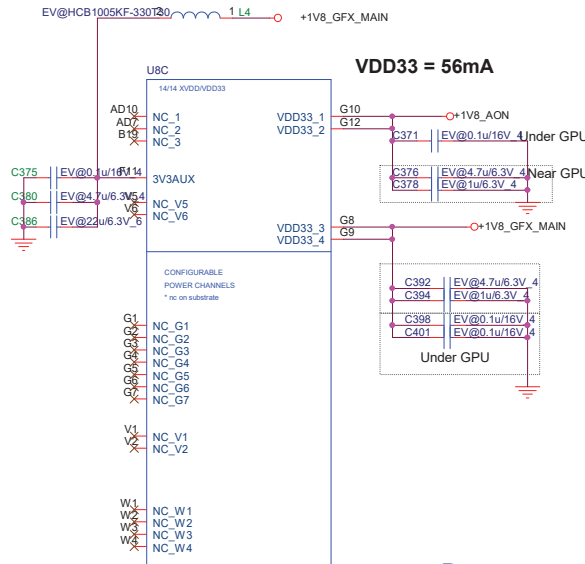
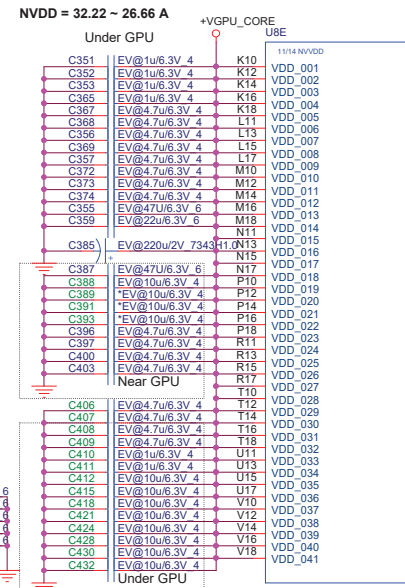
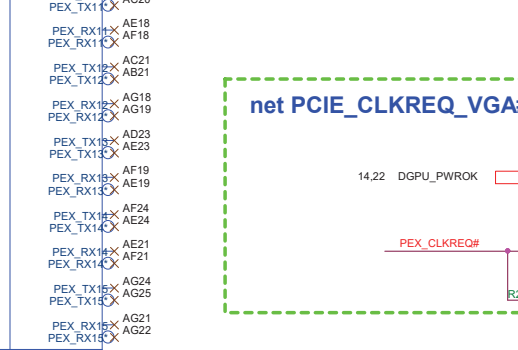
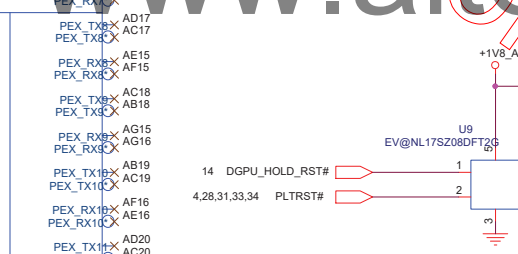
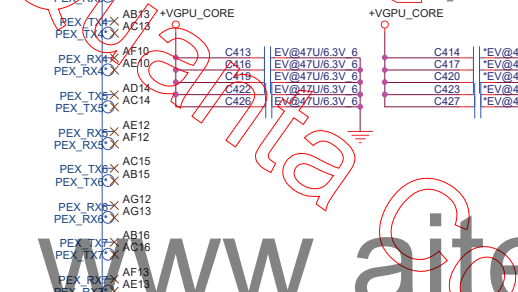
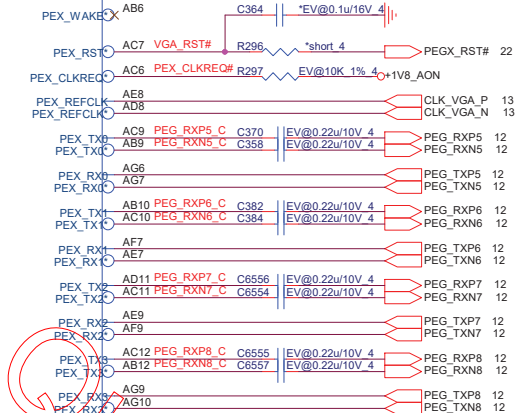
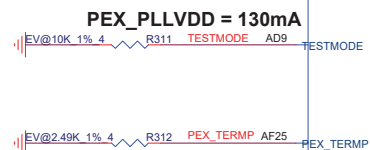
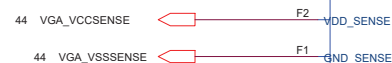
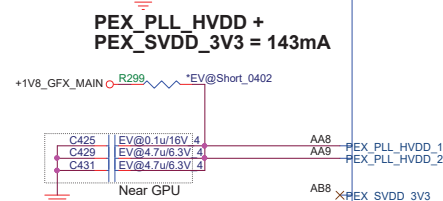
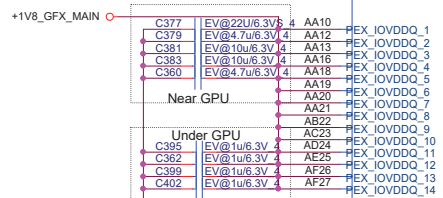
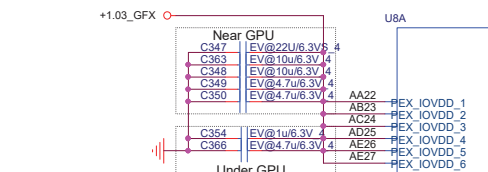


| Memory 8G & Memory 16G TABLE | | | |
|------------------------------|-----------------|------------------|--|
| | Memory 8G | Memory 16G | |
| R278 | 0Q CS000002JB38 | 240Q CS12402FB03 | |
| R279 | 0Q CS000002JB38 | 240Q CS12402FB03 | |
| R280 | 0Q CS000002JB38 | 240Q CS12402FB03 | |
| R281 | 0Q CS000002JB38 | 240Q CS12402FB03 | |
| R282 | UNINSTAL | INSTAL | |
| R283 | UNINSTAL | INSTAL | |
| R284 | UNINSTAL | INSTAL | |
| R285 | UNINSTAL | INSTAL | |
| R290 | INSTAL | UNINSTAL | |
| R291 | INSTAL | UNINSTAL | |
| R292 | INSTAL | UNINSTAL | |
| R293 | INSTAL | UNINSTAL | |

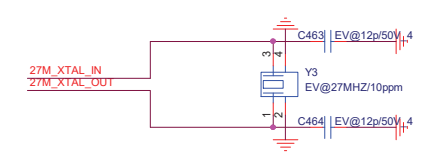


Place these Caps near Channel B
1uF/0.01uF 1pcs on each side of connector











MF=0 Non-mirrored

Channel 0 MF=0 Non-mirrored

CHANNEL A: 2G/4G GDDR5

Channel 0 MF=0 Non-mirrored

23

QD24~31

QD16~23

QD8~15

QD0~7

QD40~47

QD32~39

QD56~63

QD48~55

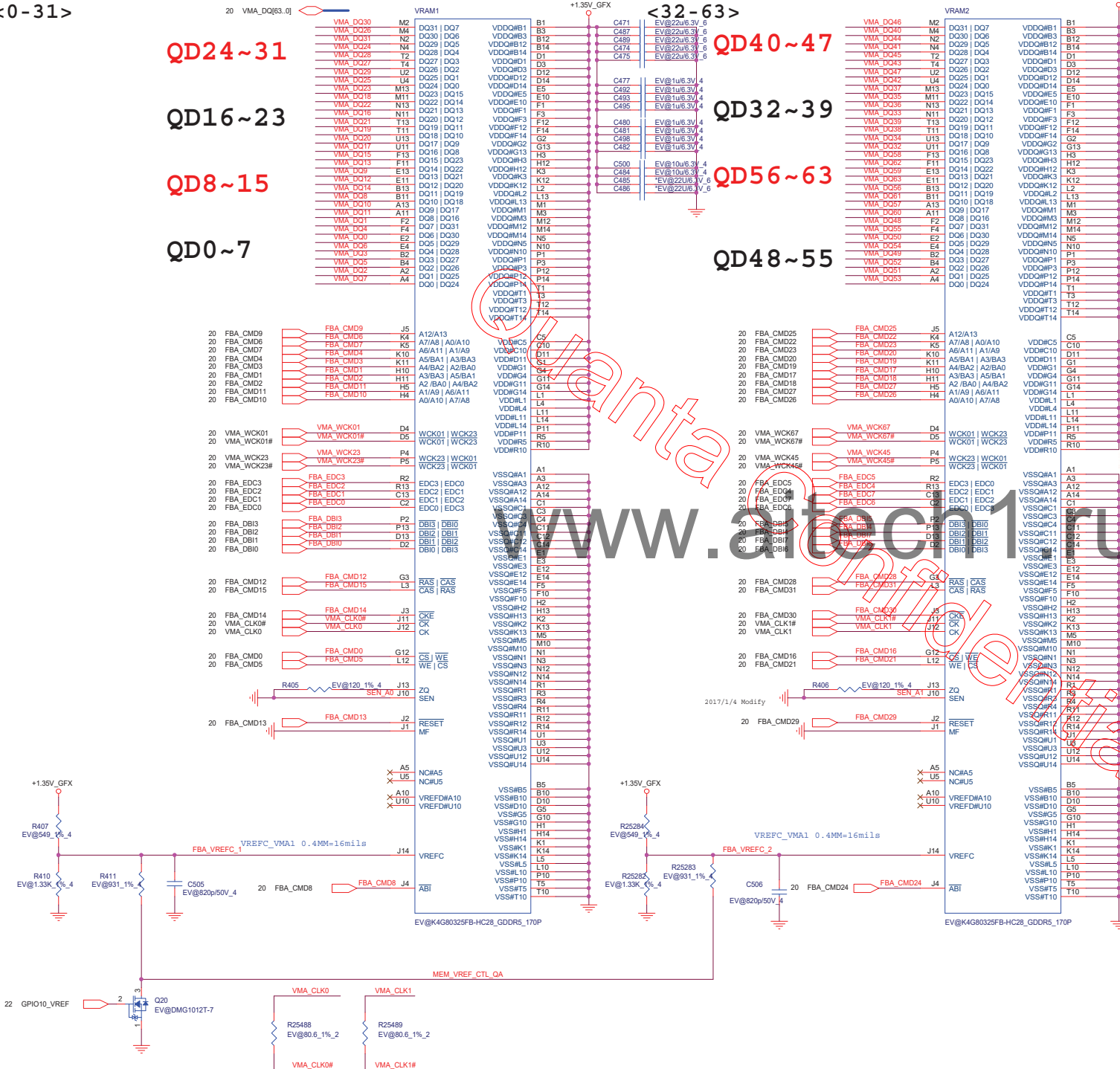
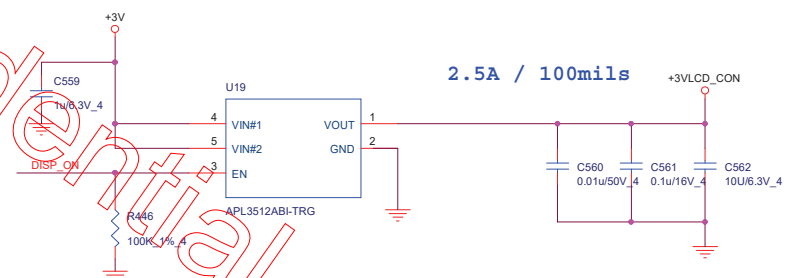


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

| Command Ball on GPU | | DRAM Signal Definition | |
|-----------------------------|-------------------------------|------------------------|--|
| For DRAM(s) tied to DQ[3:0] | For DRAM(s) tied to DQ[63:32] | | |
| FBA_CMD0 | FBA_CMD16 | CS* | |
| FBA_CMD1 | FBA_CMD17 | A3_BA3 | |
| FBA_CMD2 | FBA_CMD18 | A2_BA0 | |
| FBA_CMD3 | FBA_CMD19 | A4_BA2 | |
| FBA_CMD4 | FBA_CMD20 | A5_BA1 | |
| FBA_CMD5 | FBA_CMD21 | WE* | |
| FBA_CMD6 | FBA_CMD22 | A7_A8 | |
| FBA_CMD7 | FBA_CMD23 | A6_A11 | |
| FBA_CMD8 | FBA_CMD24 | AB1* | |
| FBA_CMD9 | FBA_CMD25 | A12_RFU | |
| FBA_CMD10 | FBA_CMD26 | A0_A10 | |
| FBA_CMD11 | FBA_CMD27 | A1_A9 | |
| FBA_CMD12 | FBA_CMD28 | RAS* | |
| FBA_CMD13 | FBA_CMD29 | RST* | |
| FBA_CMD14 | FBA_CMD30 | CKE* | |
| FBA_CMD15 | FBA_CMD31 | CAS* | |

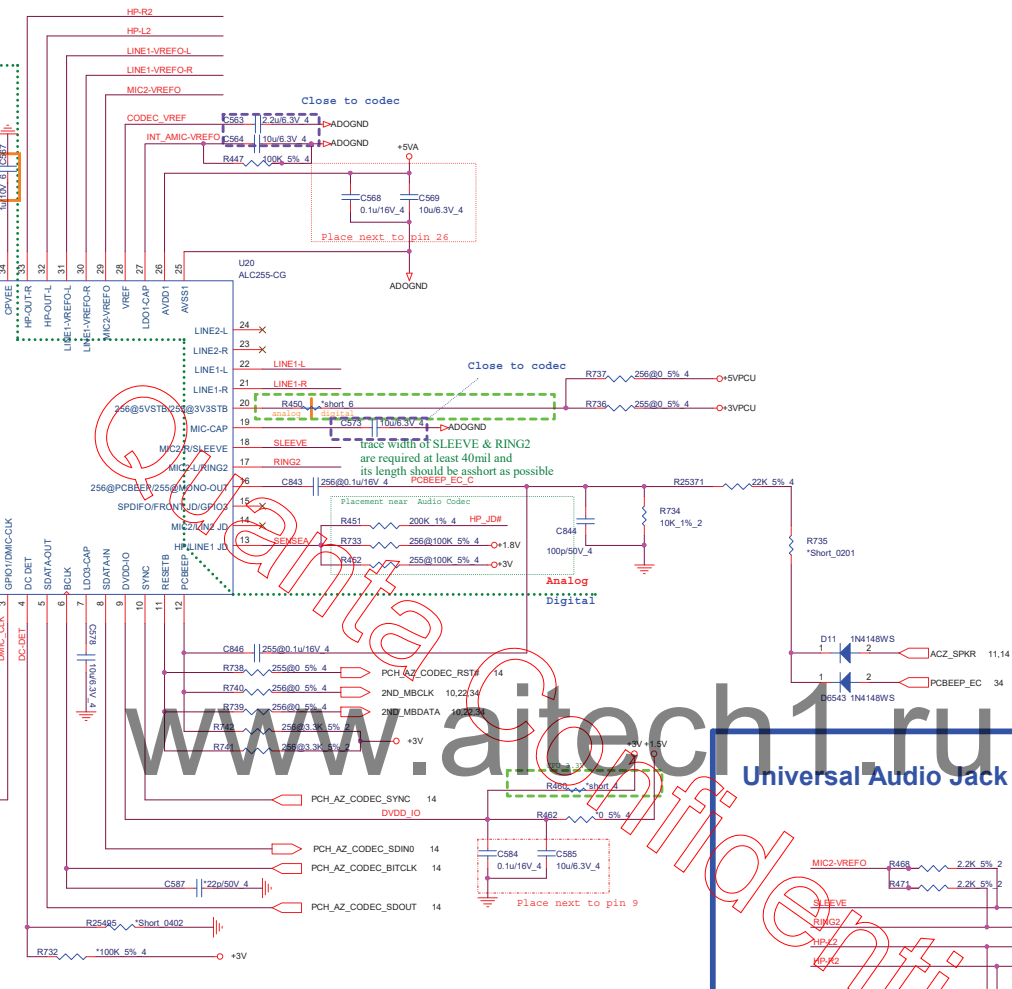
Table 9.5 GDDR5 DEBUG Command Lines

| Command Ball on GPU | DRAM Signal Definition |
|------------------------------------|------------------------|
| FBA_CMD32 (do not connect to DRAM) | (not used) |
| FBA_CMD33 (do not connect to DRAM) | (not used) |
| FBA_CMD34 (do not connect to DRAM) | DEBUG0 |
| FBA_CMD35 (do not connect to DRAM) | DEBUG1 |



PCH
PCH_LVDS_BL
34 PCH_BLO
EC

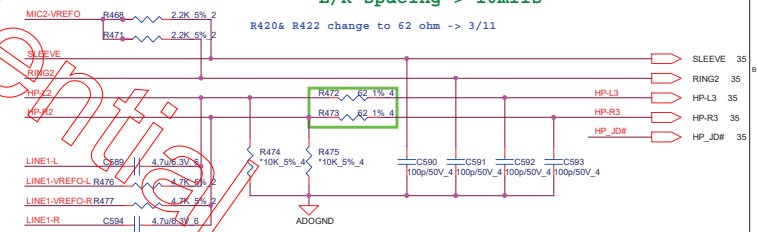
The diagram illustrates the PCB layout for the HCB1608KF-121T30 AVDD2 pin. It shows the placement of components R448, R449, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R7

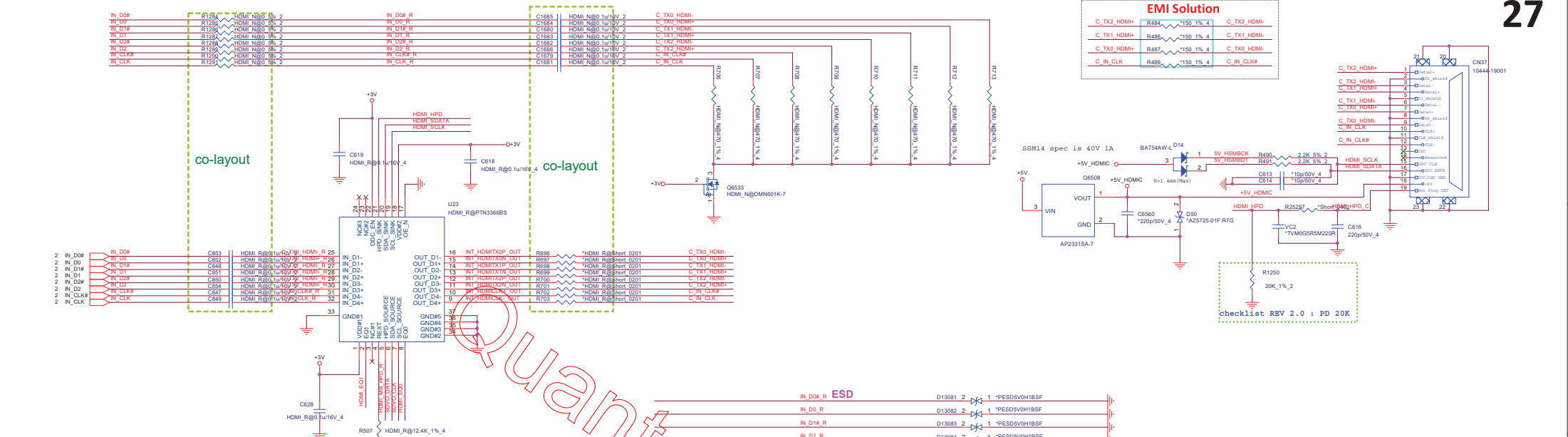


The diagram illustrates a differential signal line layout. A vertical line separates the **DIGITAL** section (left) from the **ANALOG** section (right). In the digital section, a +5V supply is connected to a network of capacitors C596 and C597, which are connected to ground. The analog section features a +5VIA supply connected to capacitors C598 and C599, which are connected to ADOGND. A center tap, labeled L16, connects the two sections at the midpoint of the signal line.

[illegible]

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils



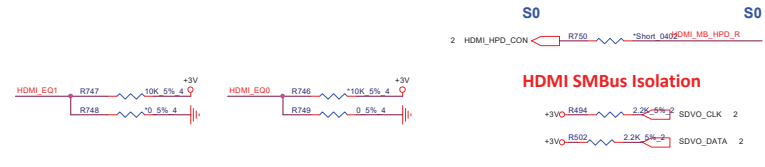


HDMI

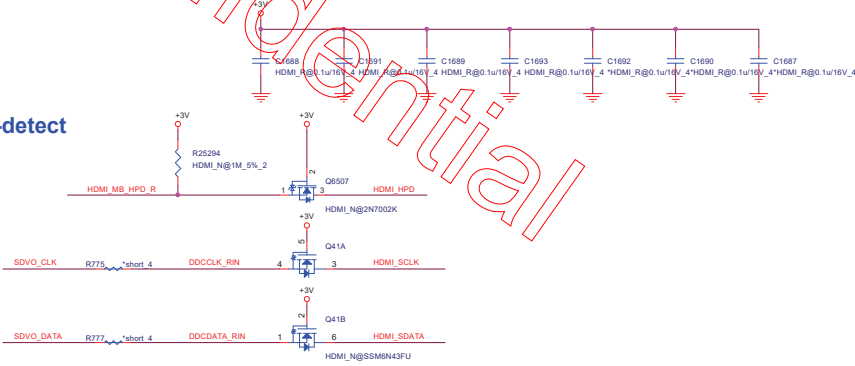
| OE_N | DDC_EN | HPD_SINK | Source output | PTN3366 power mode |
|------|--------|------------|---------------|-------------------------|
| LOW | HIGH | HIGH | source active | Active mode; DDC active |
| LOW | LOW | LOW | don't care | Standby mode |
| HIGH | LOW | don't care | don't care | Ultra low-power mode |

The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

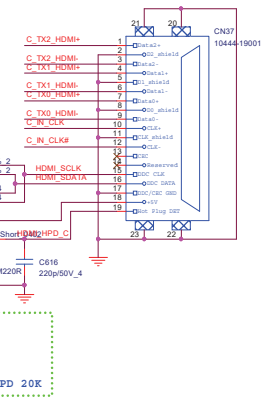
| Table 5. Equalizer settings | | |
|-----------------------------|--------------------------|---------------------------|
| Inputs | | Equalization for 3 Gbit/s |
| EQ1 | EQ0 | |
| short to GND | short to GND | 0 dB |
| short to GND | short to V _{DD} | 2 dB |
| short to V _{DD} | short to GND | 4 dB |
| short to V _{DD} | short to V _{DD} | 6 dB |



HDMI-detect



| EMI Solution | | |
|--------------|------|----------|
| C TX2 HDMI+ | R484 | 150 1% 4 |
| C TX1 HDMI+ | R485 | 150 1% 4 |
| C TX0 HDMI+ | R487 | 150 1% 4 |
| C IN_CLK | R489 | 150 1% 4 |

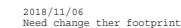
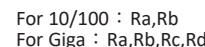


* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

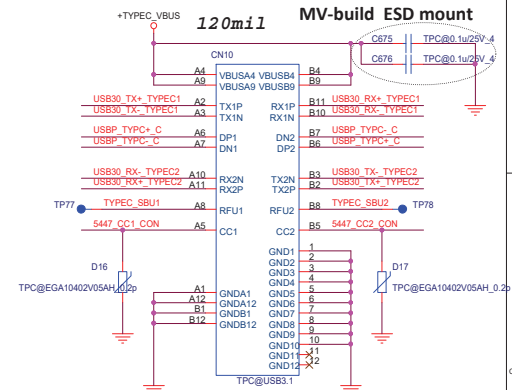
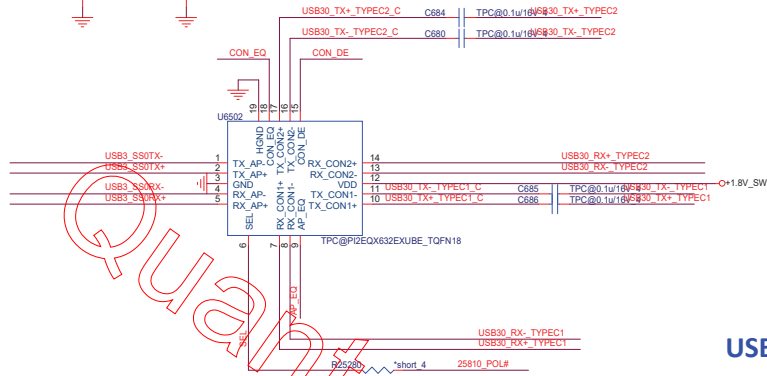
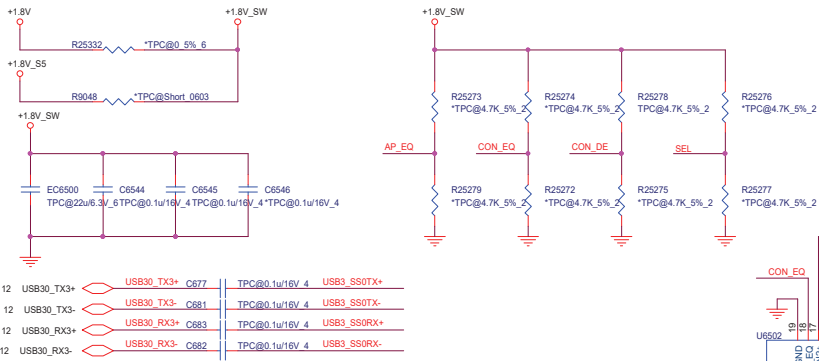
* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)



+3V_S5



TYPE C and MUX PI2EQX632EXUBE

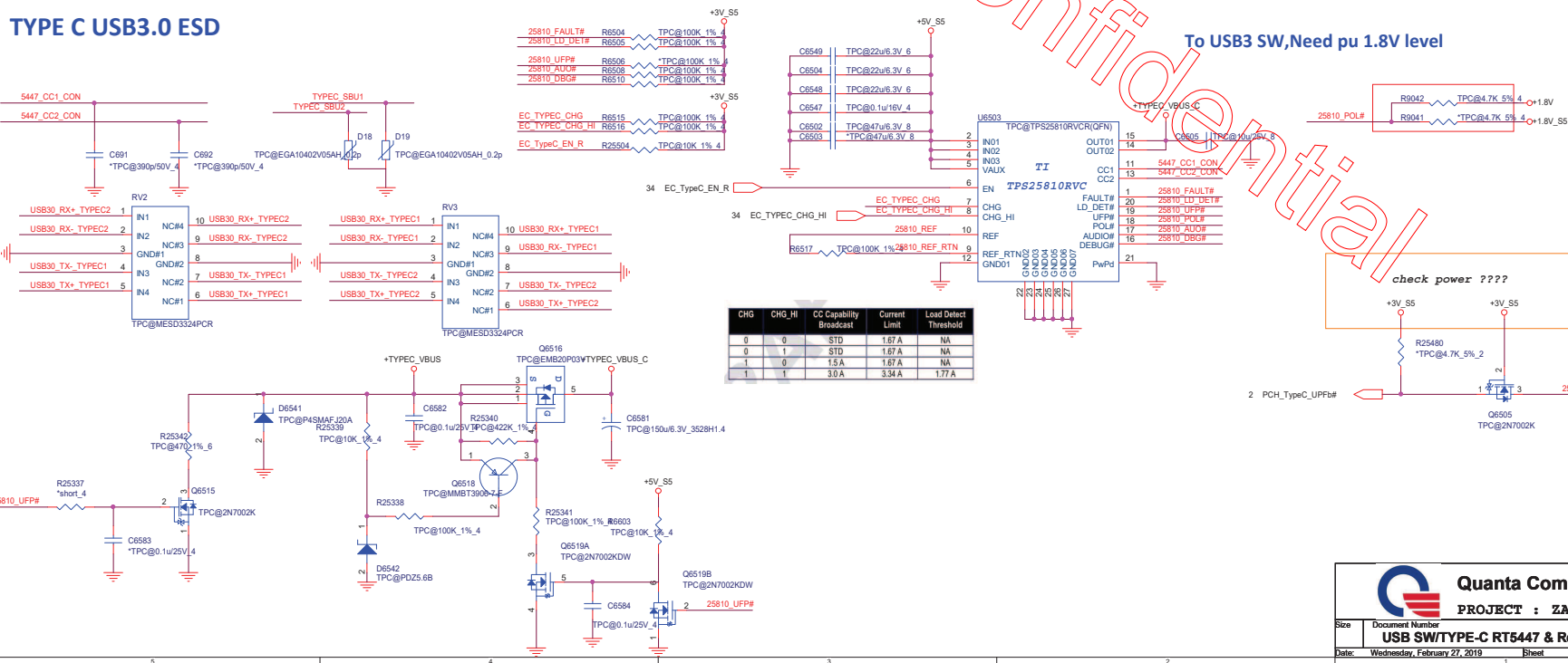


USB2.0

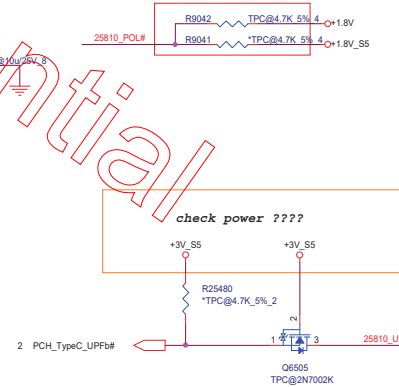


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TYPE C USB3.0 ESD

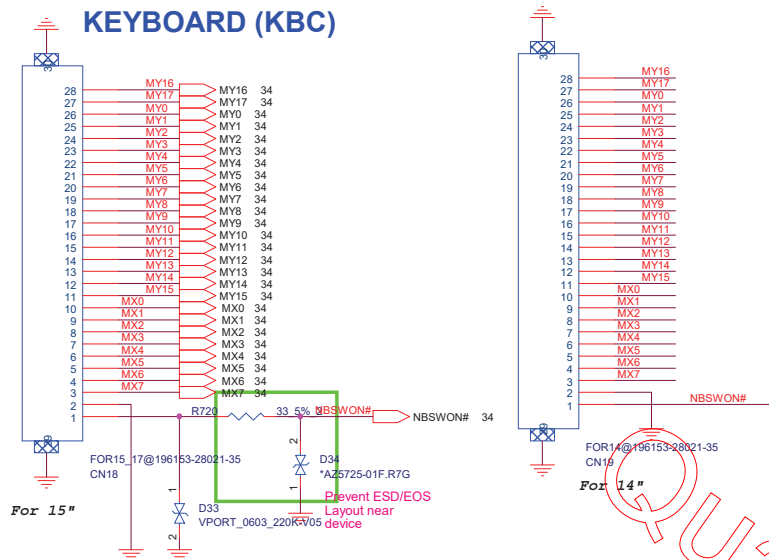


To USB3 SW,Need pu 1.8V level

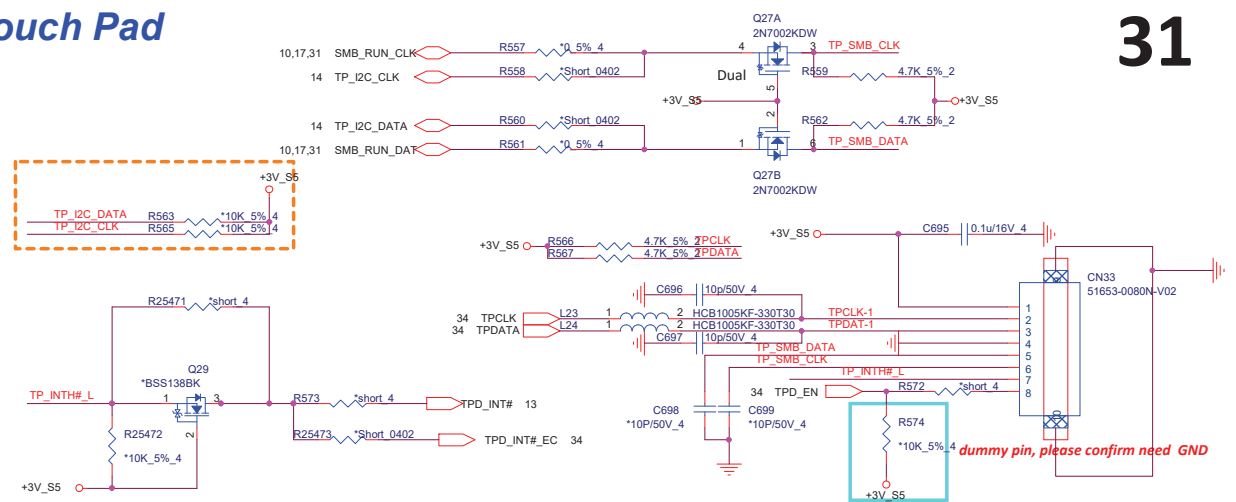


| CHG | CHG_HI | CC Capability Broadcast | Current Limit | Load Detect Threshold |
|-----|--------|-------------------------|---------------|-----------------------|
| 0 | 0 | STD | 1.67 A | NA |
| 0 | 1 | STD | 1.67 A | NA |
| 1 | 0 | 1.5 A | 1.67 A | NA |
| 1 | 1 | 3.0 A | 3.34 A | 1.77 A |

KEYBOARD (KBC)

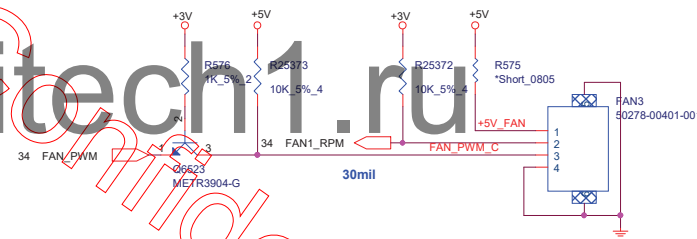


Touch Pad



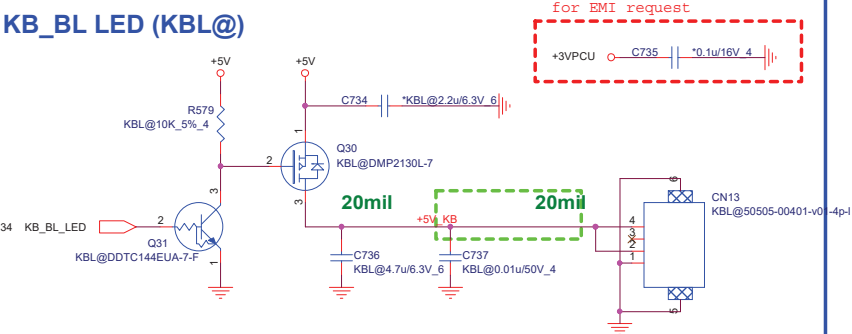
31

FAN check pin define

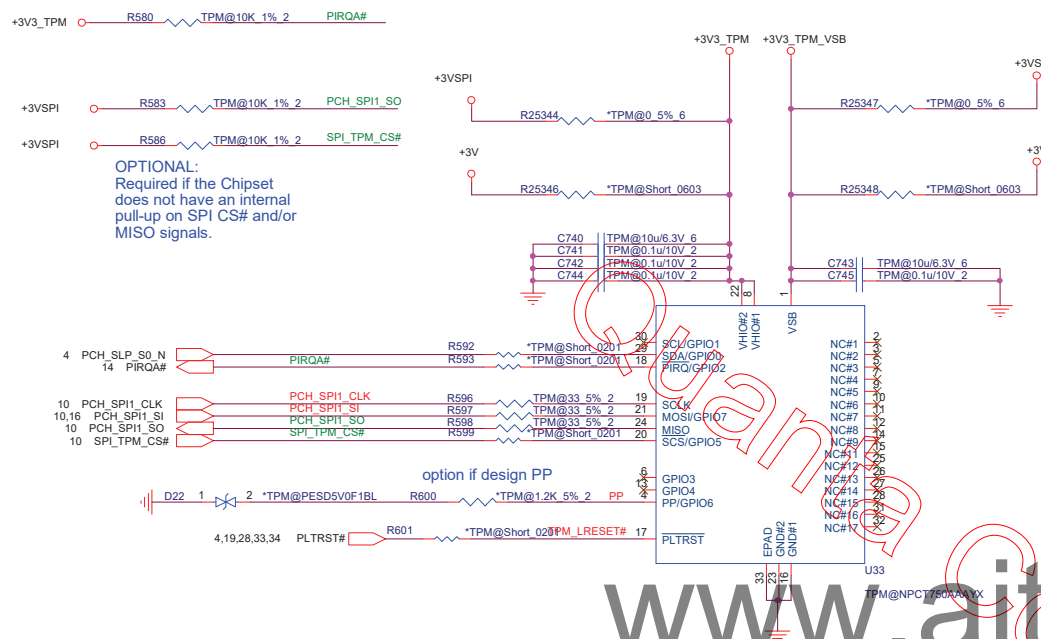


| | | | |
|------|------|----------|---|
| MY5 | C707 | 220p/25V | 2 |
| MY6 | C706 | 220p/25V | 2 |
| MY3 | C708 | 220p/25V | 2 |
| MY7 | C709 | 220p/25V | 2 |
| MY8 | C711 | 220p/25V | 2 |
| MY9 | C713 | 220p/25V | 2 |
| MY10 | C714 | 220p/25V | 2 |
| MY11 | C715 | 220p/25V | 2 |
| MY1 | C716 | 220p/25V | 2 |
| MY2 | C717 | 220p/25V | 2 |
| MY4 | C718 | 220p/25V | 2 |
| MY0 | C719 | 220p/25V | 2 |
| MX4 | C720 | 220p/25V | 2 |
| MX6 | C721 | 220p/25V | 2 |
| MX3 | C722 | 220p/25V | 2 |
| MX2 | C723 | 220p/25V | 2 |
| MX7 | C724 | 220p/25V | 2 |
| MX0 | C725 | 220p/25V | 2 |
| MX5 | C726 | 220p/25V | 2 |
| MX1 | C727 | 220p/25V | 2 |
| MY12 | C728 | 220p/25V | 2 |
| MY13 | C729 | 220p/25V | 2 |
| MY14 | C730 | 220p/25V | 2 |
| MY15 | C731 | 220p/25V | 2 |
| MY16 | C732 | 220p/25V | 2 |
| MY17 | C733 | 220p/25V | 2 |

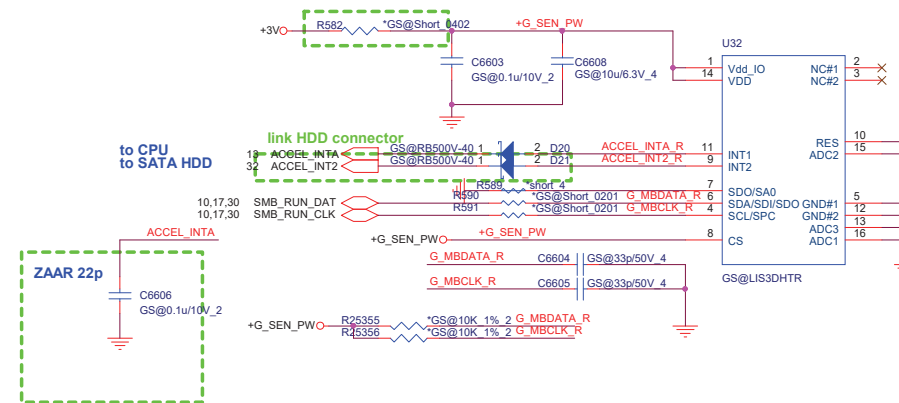
KB_LED (KBL@)



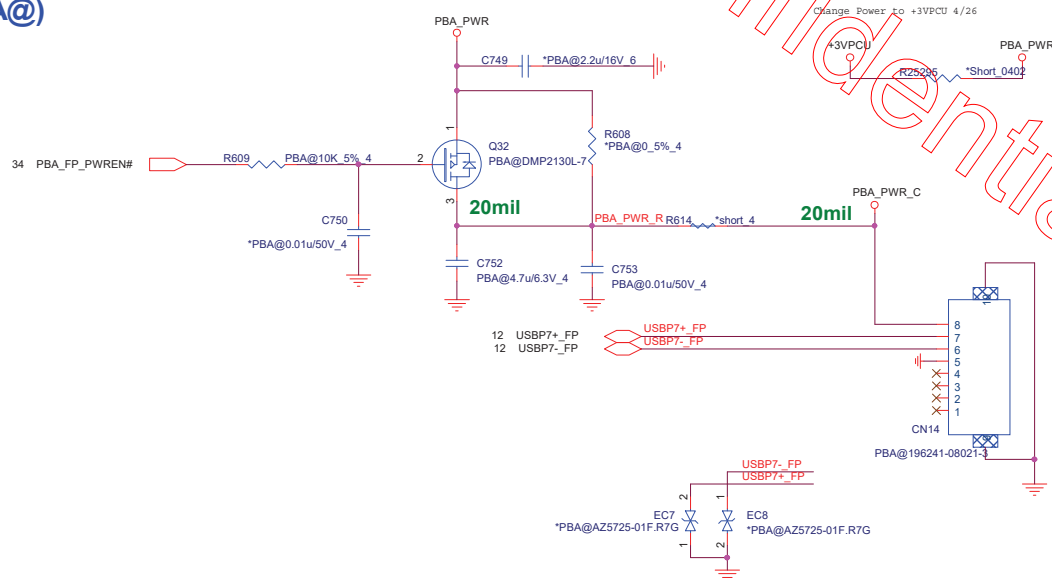
TPM NPCT750



G-sensor (GS@)

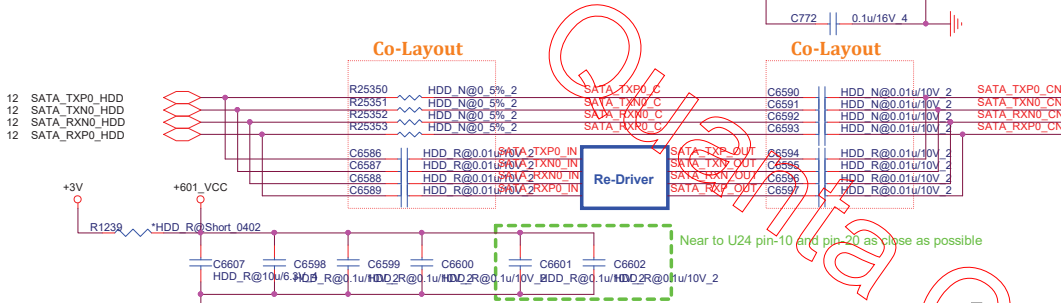
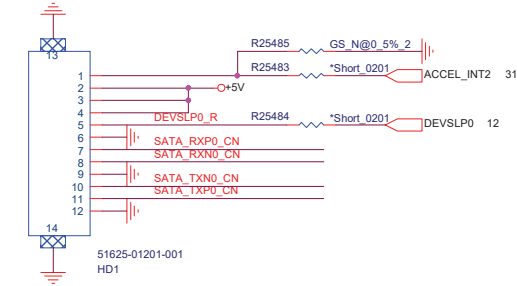


PBA (PBA@)



SATA HDD & LED

24,29,35,37,39,40,41,42,44,45,46 +5V_S5
25,26,27,30,37,43 +5V
2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,33,34,35,37,38,39,40,43,44,45,46 +3V
2,4,10,12,13,14,15,28,29,30,33,34,37,39,43 +3V_S5
9,15,38 +1.05V_DEEP_SUS



SATA HDD Re-driver

| | |
|---------|----------|
| BQ2 | H - 14dB |
| X - 0dB | |
| L - 7dB | |

| | |
|---------|----------|
| BQ1 | H - 14dB |
| X - 0dB | |
| L - 7dB | |

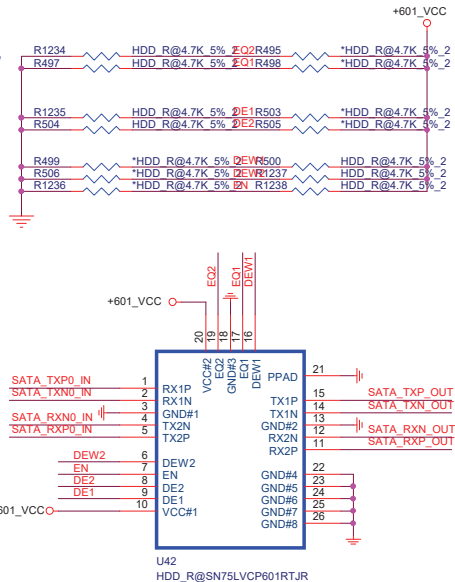
| | |
|--------------------|-------------------|
| DEW1 | H - Long Duration |
| X - NC (Long) | |
| L - Short Duration | |

| | |
|----------|----------|
| DE1 | H - -2dB |
| X - -4dB | |
| L - 0dB | |

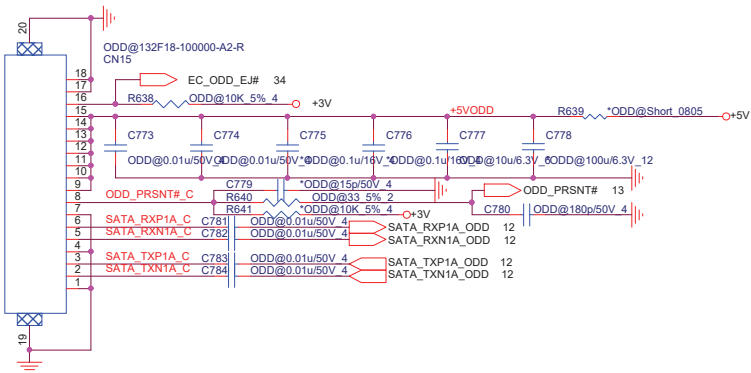
| | |
|----------|----------|
| DE2 | H - -2dB |
| X - -4dB | |
| L - 0dB | |

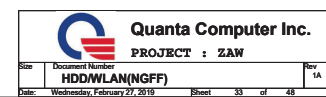
| | |
|--------------------|-------------------|
| DEW2 | H - Long Duration |
| X - NC (Long) | |
| L - Short Duration | |

| | |
|------------------|--|
| SW7 - EN | |
| H - Enabled | |
| L - Standby Mode | |

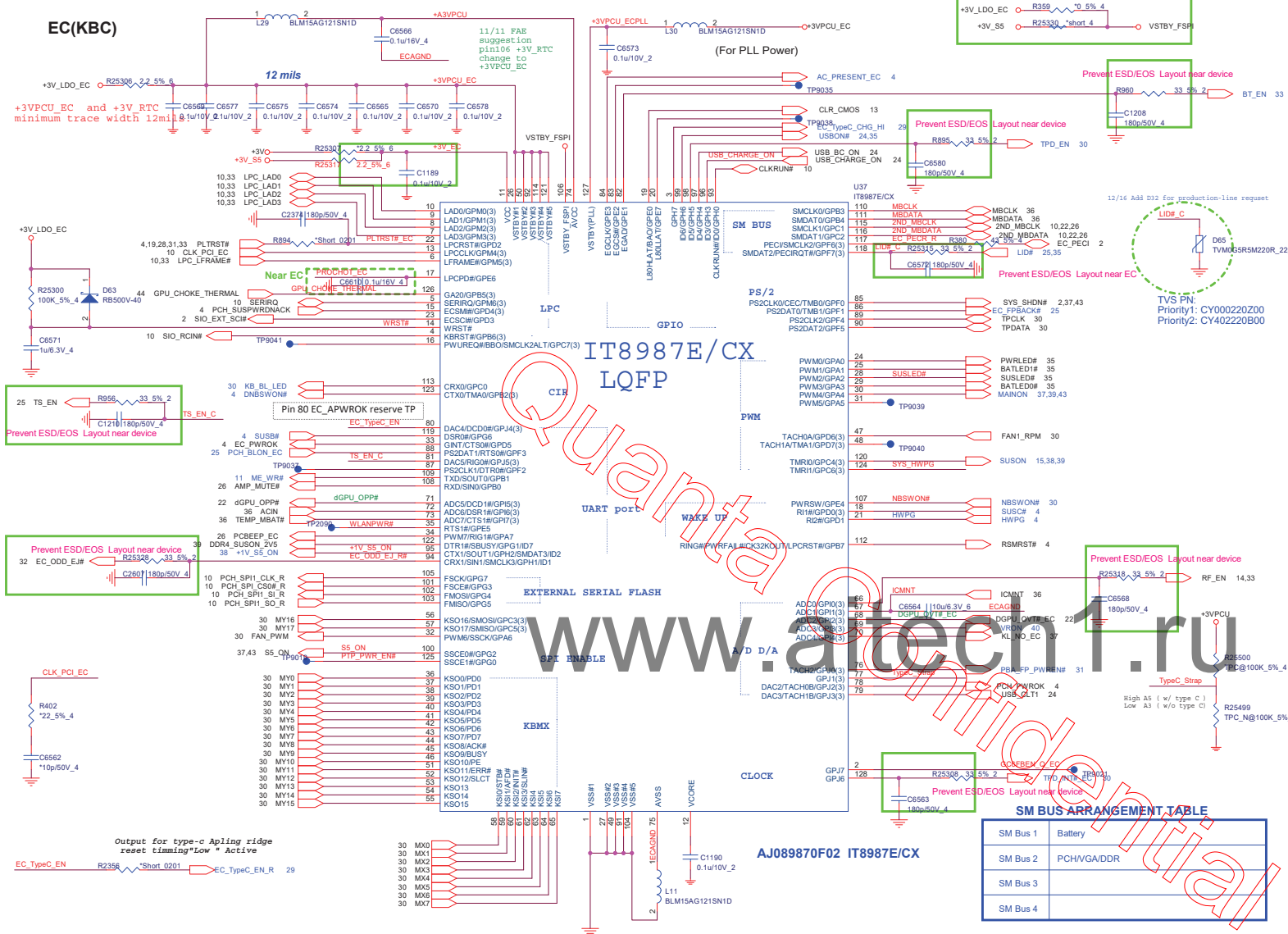


SATA ODD (ODD@)

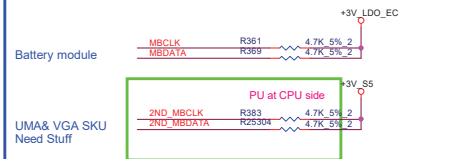




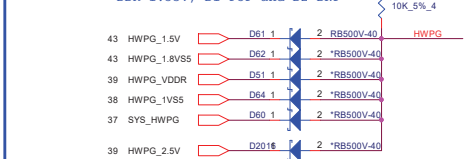
EC(KBC)



SM BUS PU(KBC)

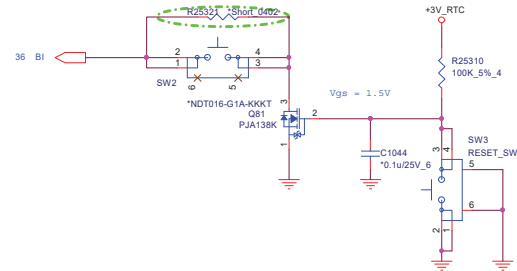


HWPG(KBC)

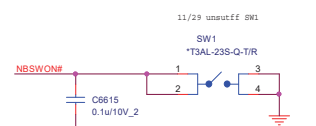


Reset SW (FSW)

Battery Detect Switch

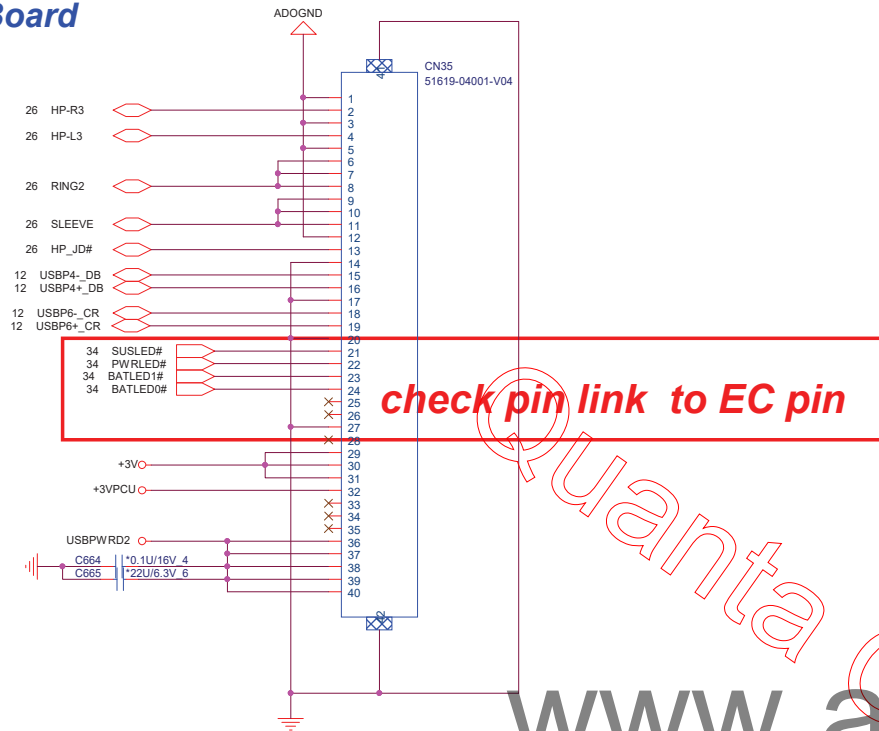


Reserve switch for test
(MP remove)

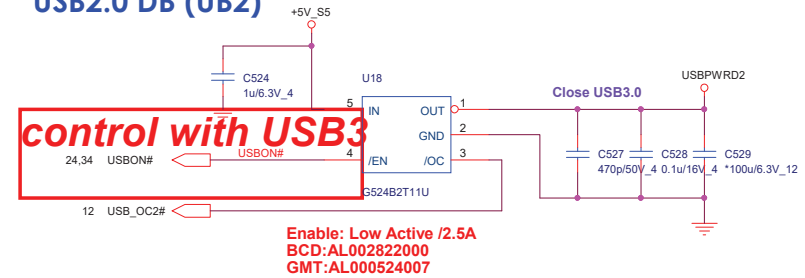


Reserve switch for test
(MP remove)

USB Board

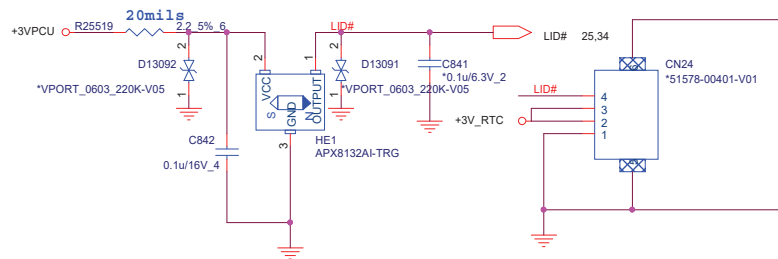


USB2.0 DB (UB2)

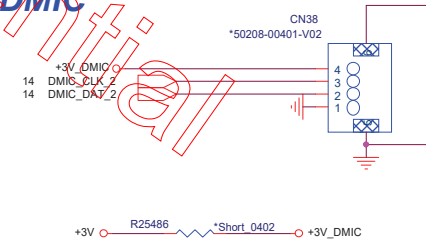


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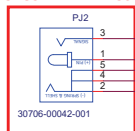
Hall Sensor



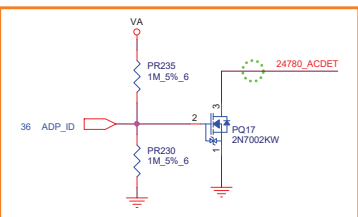
DMIC



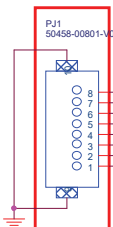
Quanta Computer Inc.
PROJECT : ZAW



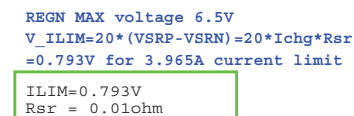
| | | |
|-------------|--------------------------|--------------------------|
| PR23 | UMA | DIS |
| | 41.2K Ohm CS34122FB19 | 33.2K Ohm CS33322FB13 |
| | 78W | 95W |



CS34122FB19 RES CHIP 41.2K 1/16W +-1%(0402) For 78W PR23



Double Check BATT Connector with ME







+1V_S5
1.0 Volt +/- 5%
TDC : 8.09A
Width : 340mil

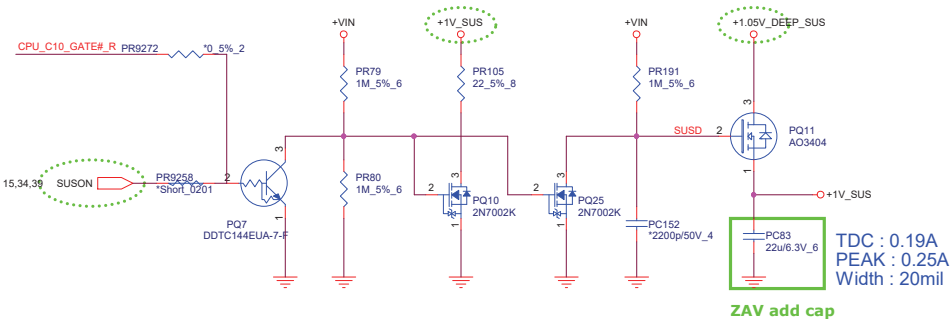
$$V_o = 0.8 \cdot (R_1 + R_2) / R_2 = 1.0V$$

VFB=0.8V

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Follow ZAV + VCCIO design

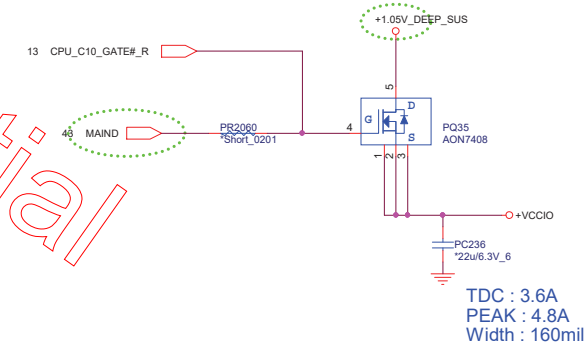
Delete



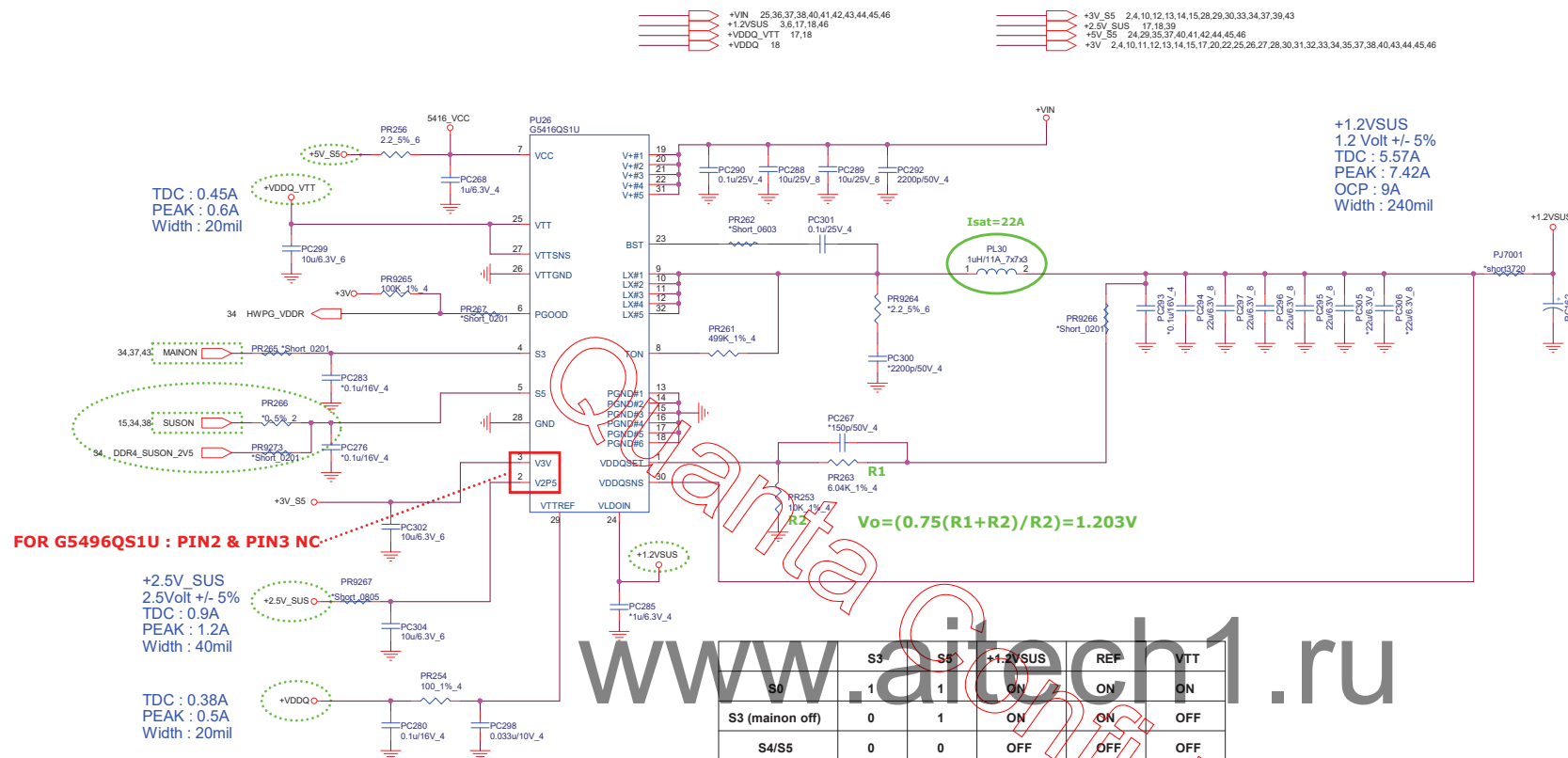
ZAV add cap

13 CPU_C10_G

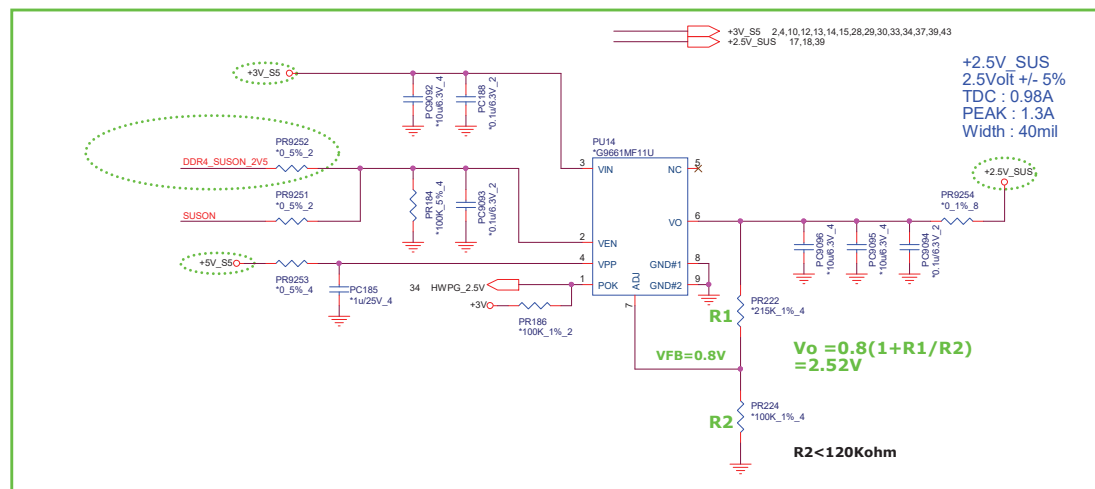
48 MAIN



TDC : 3.6A
PEAK : 4.8A
Width : 160mil



+2.5VSUS Power Rail For DDR4



31A for ICCMAX=1'

6A for ICCMAX=1V

A for ICCMAX=1V

[illegible]

Place Close to V_{DD} MOSFET

C7000
22m/25V 4

[illegible]

| | |
|-------------------|-----------|
| RGND_CORE 40 | RGND_MAIN |
| CML Base/WHL U42) | |
| KBL U22/KBL U42) | |

RGND_GT 25 RGND_AUX0

44 RGND_SA

[illegible]


45V S5

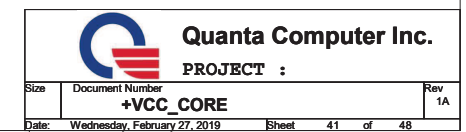
*Short_0201

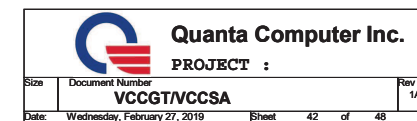
41,42 3602_DRC

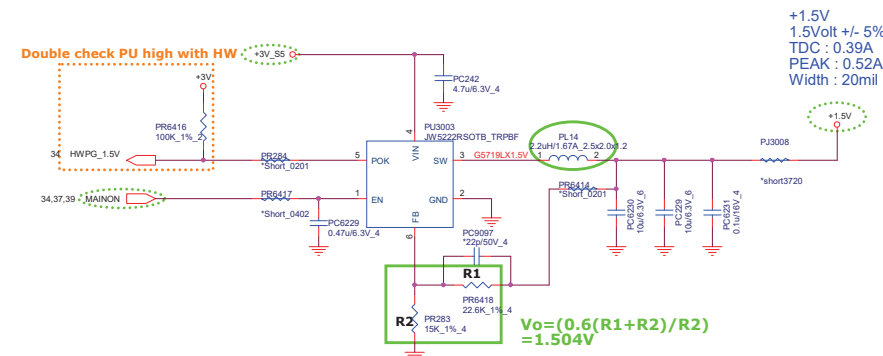
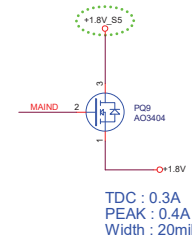
Default Settings

| KBL - R (U22/U42) | | WHL U42/CML Base |
|---|--|--|
| U22 (1+1+1 Phase) | U42 (2+1+1 Phase) | (2+1+1 Phase) |
| Vcore lcc Max : 32A lcc TDC : 21A OCP : 50A | Vcore lcc Max : 64A lcc TDC : 42A OCP : 100A | Vcore lcc Max : 70A lcc TDC : 48A OCP : 100A |
| VCCGT lcc Max : 31A lcc TDC : 18A OCP : 50A | VCCGT lcc Max : 31A lcc TDC : 12A OCP : 50A | VCCGT lcc Max : 31A lcc TDC : 18A OCP : 50A |
| VCCSA lcc Max : 6A OCP : 10A | VCCSA lcc Max : 6A OCP : 10A | VCCSA lcc Max : 6A OCP : 10A |

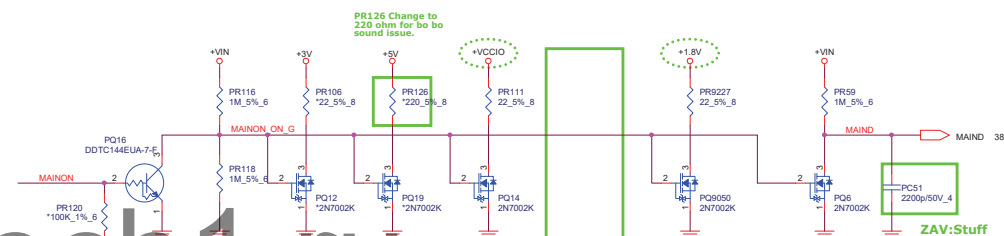
| | | |
|---|------------------------------|----------------|
|  Quanta Computer Inc. PROJECT : | | |
| Size | Document Number | Rev |
| | CPU_CORE (RT3602AJ) | |
| Date: | Wednesday, February 27, 2019 | Sheet 40 of 48 |



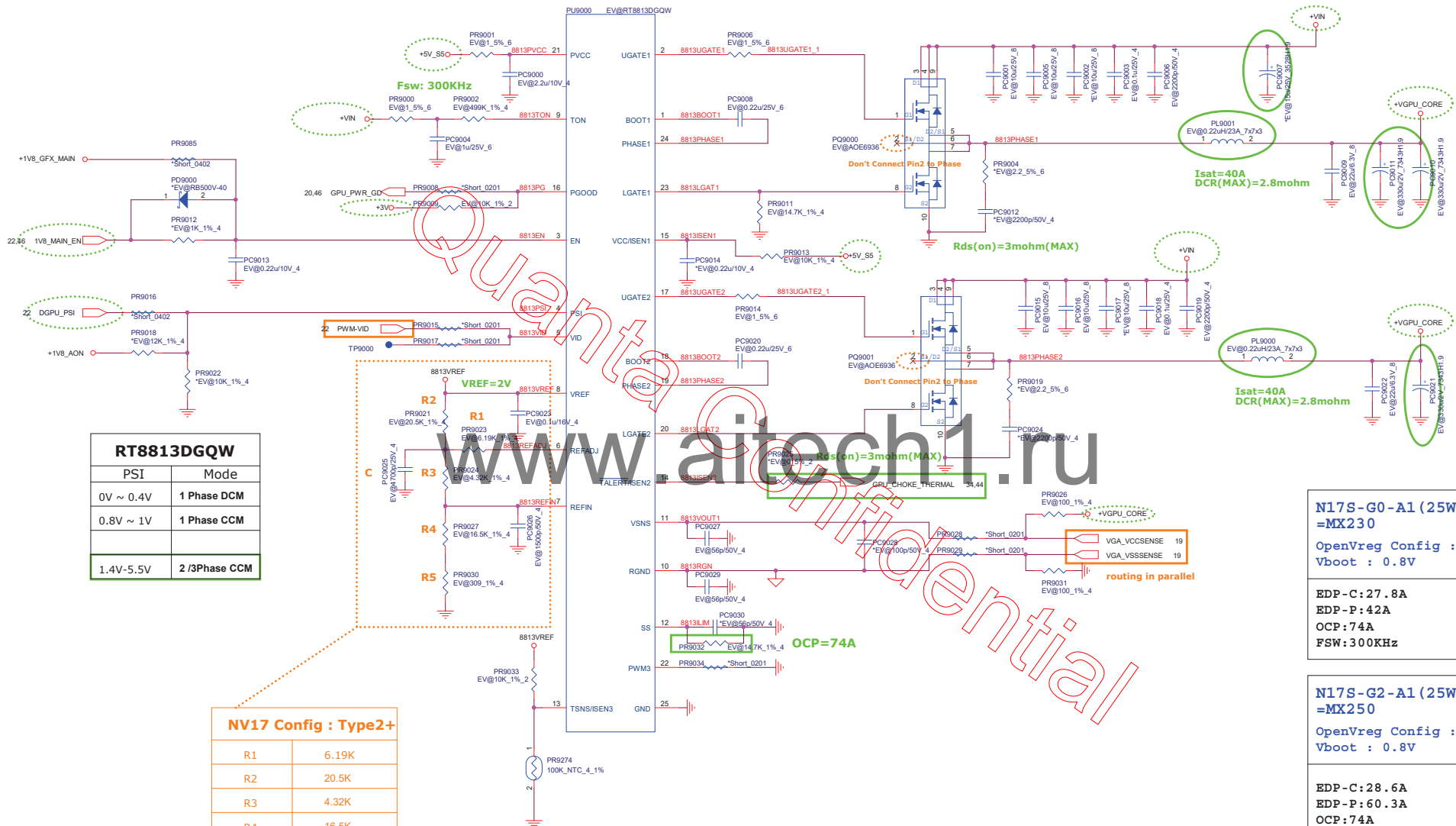




- (1) Need fine tune for thermal protect point
- (2) Note placement position
TEMP=80C



+VIN 25,36,37,38,39,40,41,42,43,45,46
 +VGPU_CORE 19
 +5V_S5 24,29,35,37,39,40,41,42,45,46
 +1V8_AON 19,21,22,46
 +1V8_GFX_MAIN 19,20,21,46
 GPU_CHOKE_THERMAL 34,44



N17S-G0-A1 (25W/GDDR5)
 =MX230

OpenVreg Config : Type2+
 Vboot : 0.8V

EDP-C: 27.8A
 EDP-P: 42A
 OCP: 74A
 FSW: 300KHz

N17S-G2-A1 (25W/GDDR5)
 =MX250

OpenVreg Config : Type2+
 Vboot : 0.8V

EDP-C: 28.6A
 EDP-P: 60.3A
 OCP: 74A
 FSW: 300KHz



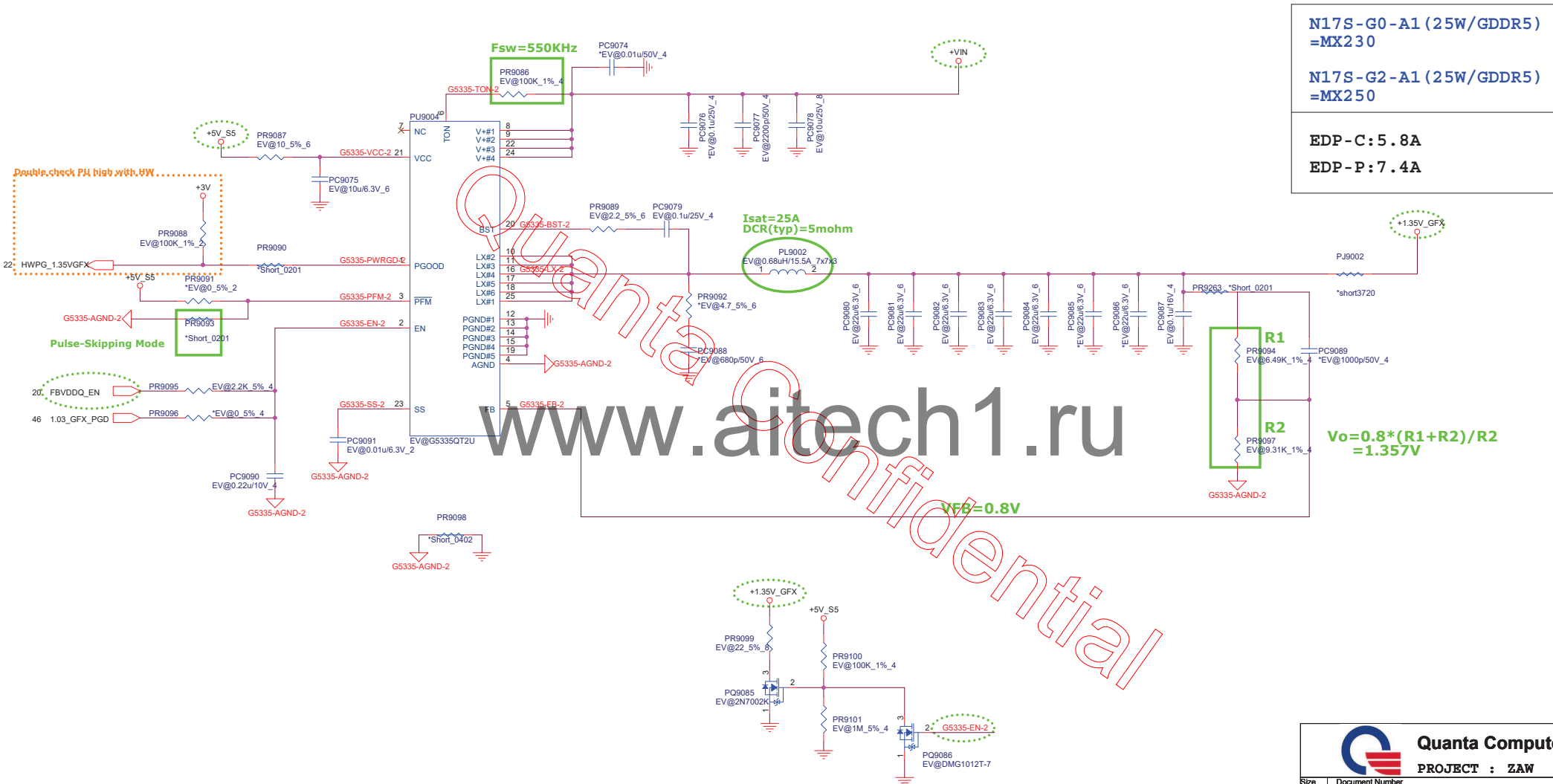
Quanta Computer Inc.
 PROJECT : ZAW

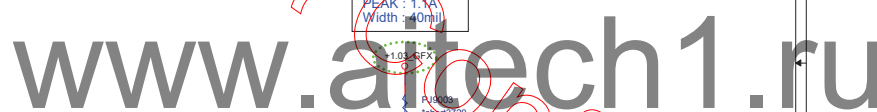
Size Document Number
 +NVVDD (RT8813DGQW)
 Date: Wednesday, February 27, 2019 Sheet 44 of 48

1.35V_GFX

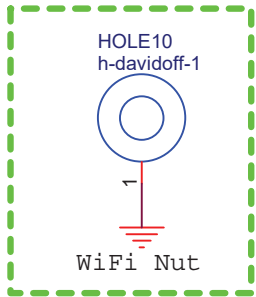
33

+VIN 25,36,37,38,39,40,41,42,43,44,46
+1.35V_GFX 20,23
+5V_S5 24,29,35,37,39,40,41,42,44,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,46

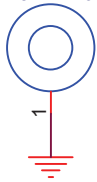




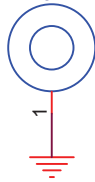
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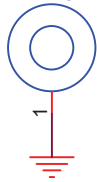
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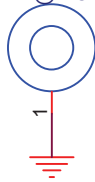
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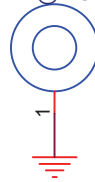
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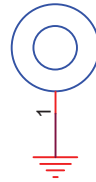
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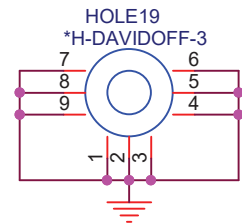
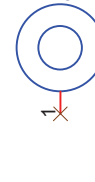
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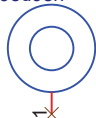
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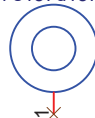
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HOLE12
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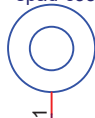
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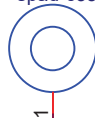
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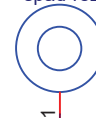
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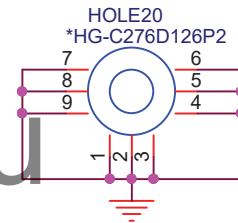
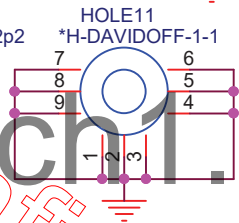
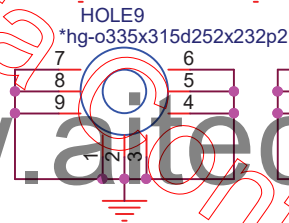
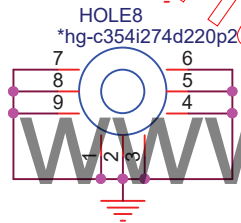
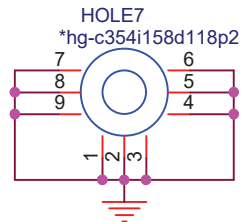
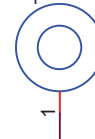
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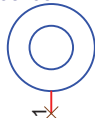
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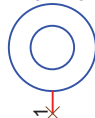
HOLE18
*spad-davidoff-1



HOLE23
*h-c98d98n



HOLE24
*h-s157d157n



Quanta Computer Inc.

PROJECT : ZAW

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| Size | Document Number | Rev |
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